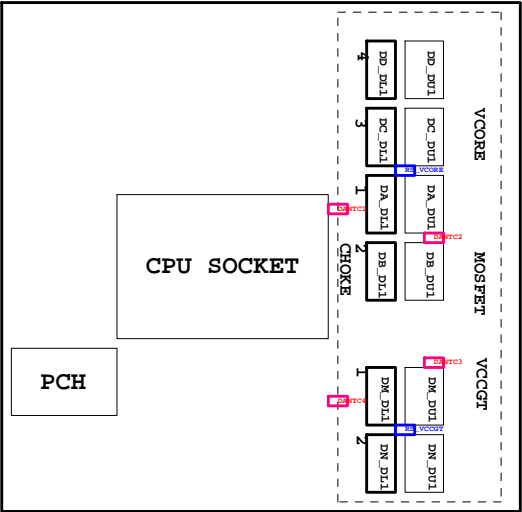


01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1151-A
05	CPU_LGA1151-B-DDR4
06	CPU_LGA1151-C
07	CPU_LGA1151-D
08	DDR 4 CHANNEL A (REV0.5)
09	DDR 4 CHANNEL B
10	PCH CLOCK BUFFER (REV0.7)
11	PCH DMI,USB,PCIE (REV0.7)
12	PCH MISC (REV0.7)
13	PCH SATA,PCIE,SATA_EXPRESS (REV0.7)
14	PCH_PWR,GND (REV0.7)
15	Dual BIOS (REV0.1)
16	I/O ITE8628 (REV1.08)
17	HWM (REV1.08)
18	FAN CTRL-SIO (REV0.7)
19	PCIEX16 SLOT
20	PCIEX4 SLOT (REV0.51)
21	PCIEX1*2 SLOT (REV0.51)
22	M.2 x4 (REV0.6)
23	SATA EXPRESS (REV0.6)
24	VCORE_ ISL95856(PWM) (REV1.0)
25	VCORE_ ISL95856(Vcore) (REV1.0)
26	VCORE_ ISL95856(VccGT) (REV1.0)
27	VCCSA_VCCIO_VCCPLL (REV0.4)
28	RT8120_DDR (REV0.88)
29	RT8120_VPP (REV0.88)
30	RT8120_PCH (REV0.67)
31	DISCRETE POWER (REV0.51)
32	NCP3933 OVER VOLTAGE
33	ATX POWER , -PROCHOT
34	KB_MS_USB (REV0.7)

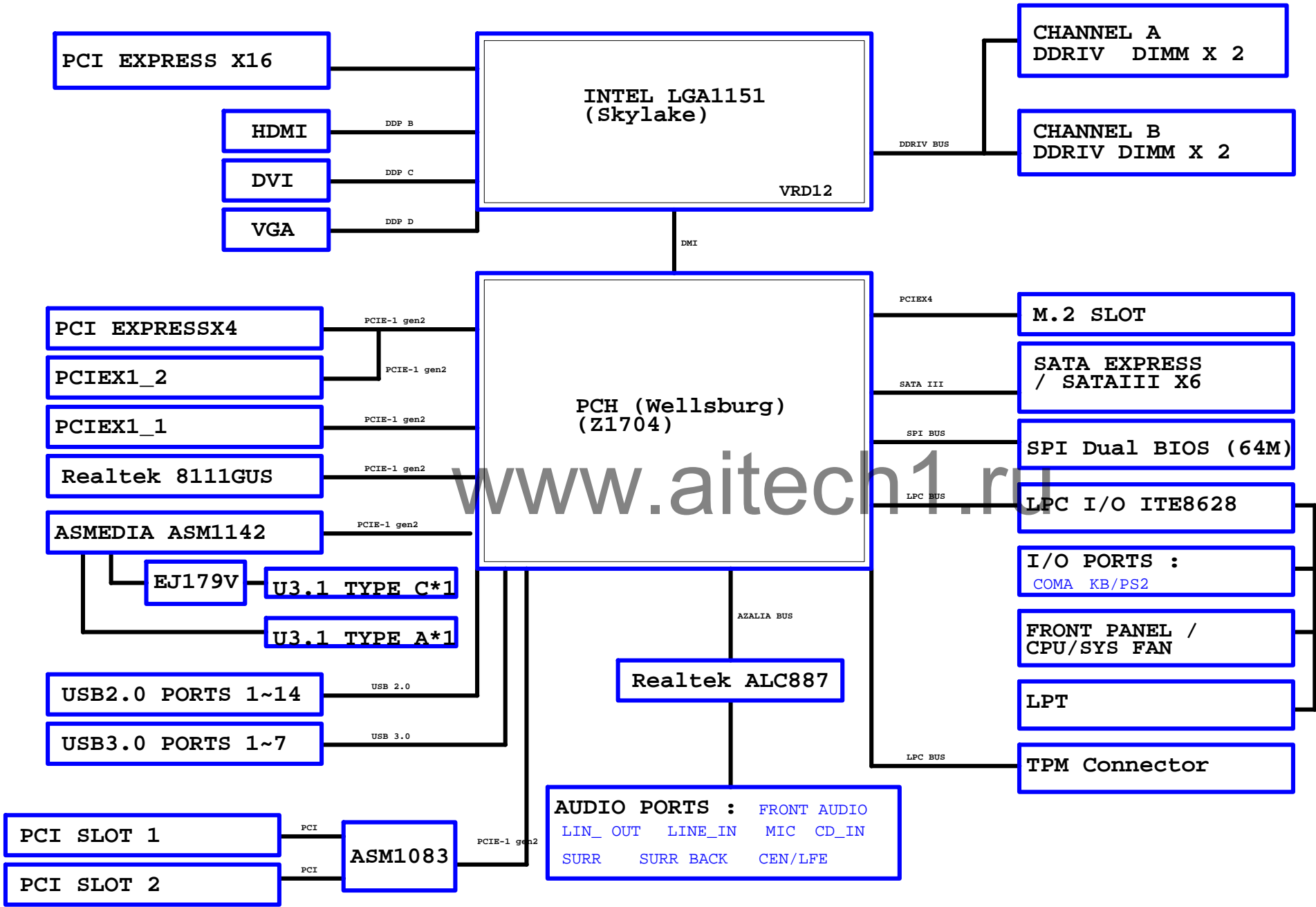
SHEET	TITLE
35	DVI (REV0.7)
36	NXP-PTN3356 - DP to VGA - IC (REV1.08)
37	NXP-PTN3356 - DP to VGA - Con (REV1.08)
38	R_USB30 (REV0.7)
39	Realtek 8111HS (REV1.06)
40	USB30_LAN CONNECTOR-8111HS (REV1.06)
41	ALC887-VD2 CODEC (REV0.7)
42	REAR AUDIO JACK (REV0.7)
43	F_USB30 (REV0.7)
44	F_USB20 (REV0.7)
45	COM , LPT , TPM , THB (REV0.7)
46	F_PANEL (REV0.7)
47	ASM1083 (REV0.9)
48	PCI SLOT 1&2 (REV0.9)
49	ASM1083 POWER (REV0.9)
50	EMI-ESD (REV0.1)
51	TABLE LIST
52	ASM1142 USB31A (REV0.63)
53	HD3SS3212&TUSB321_A (REV0.63)
54	HDMI (REV0.7)

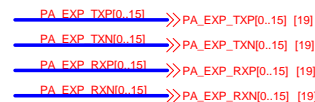
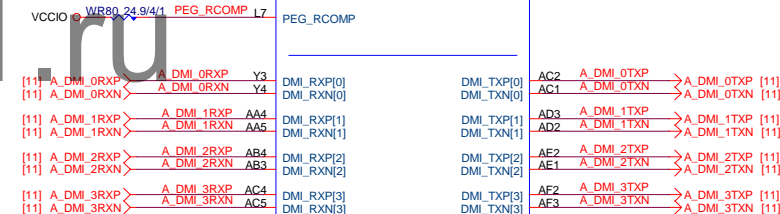
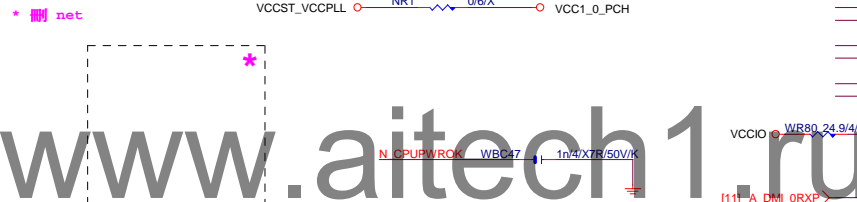
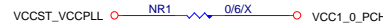
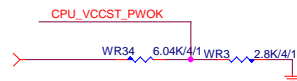
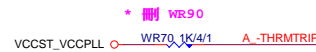
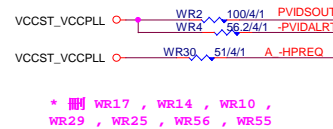


Component value change history

[illegible][illegible]

BLOCK DIAGRAM

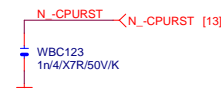




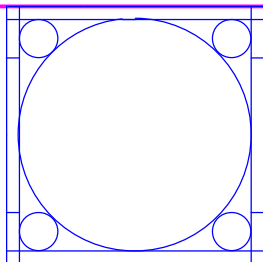
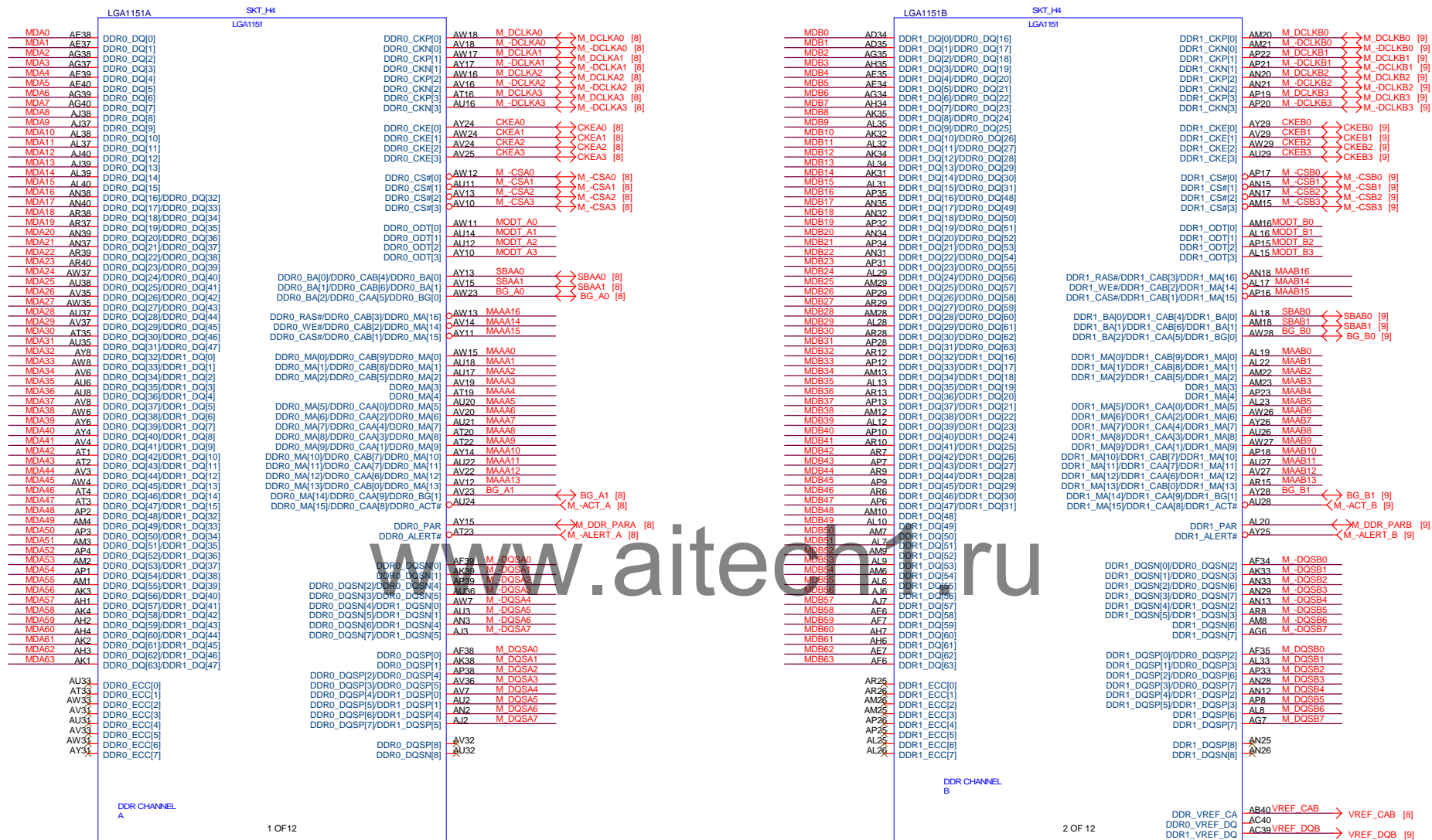
W=12 mil out of CPU
S=15 mil out of CPU

```
G-15u : (CPU-SK/1151/S/15)
10SC1-F01151-11R / 10SC1-F01151-12R
G-FL : (CPU-SK/1151/S/GF)
10SC1-F01151-21R / 10SC1-F01151-22R
```

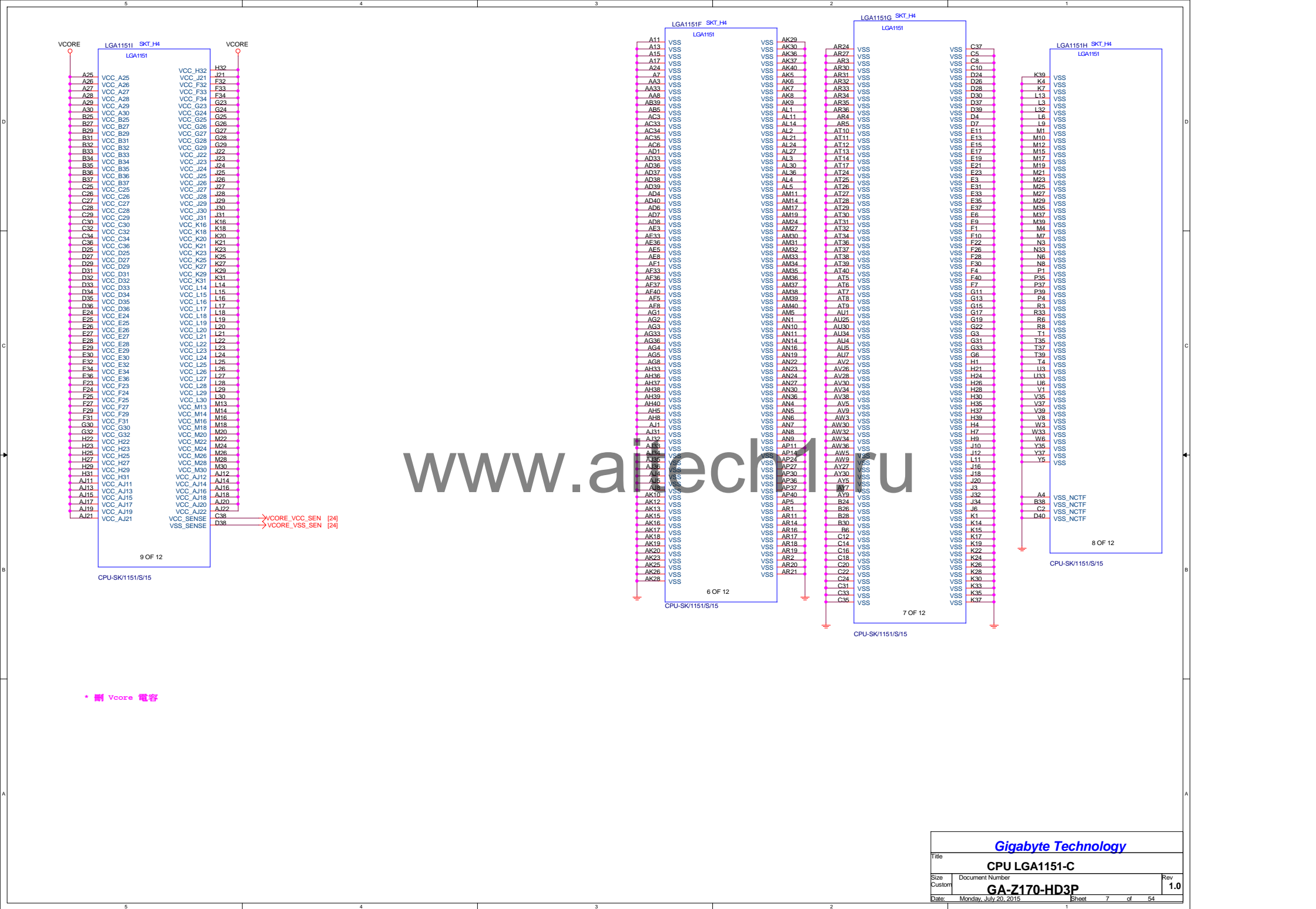
-CPURST



Bifurcation Config.	Signals Lanes		
	CFG[6]	CFG[5]	CFG[2]
1x16	1	1	1
1x16 Reversed	1	1	0
2x8	1	0	1
2x8 Reversed	1	0	0
1x8+2x4	0	0	1
1x8+2x4 Reversed	0	0	0



Need check the new CPU ME



刪除MR22 &VDDSPD SHORT PROTECT

www.aitech1.ru

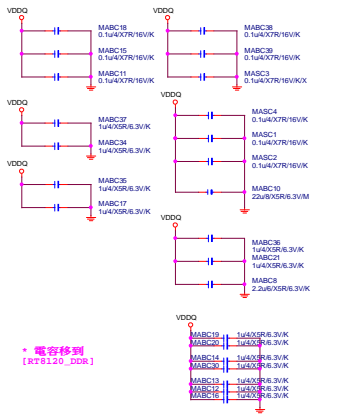
DDR4288BKV/VADG15ONE LATCH LONG

刪除 short pad
CHANNEL A0
SA2:0=000

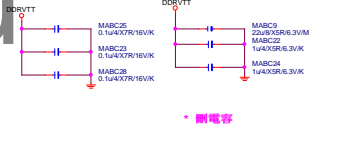
DDR4288BKV/VADG15ONE LATCH LONG

刪除 short pad
CHANNEL A1
SA2:0=001

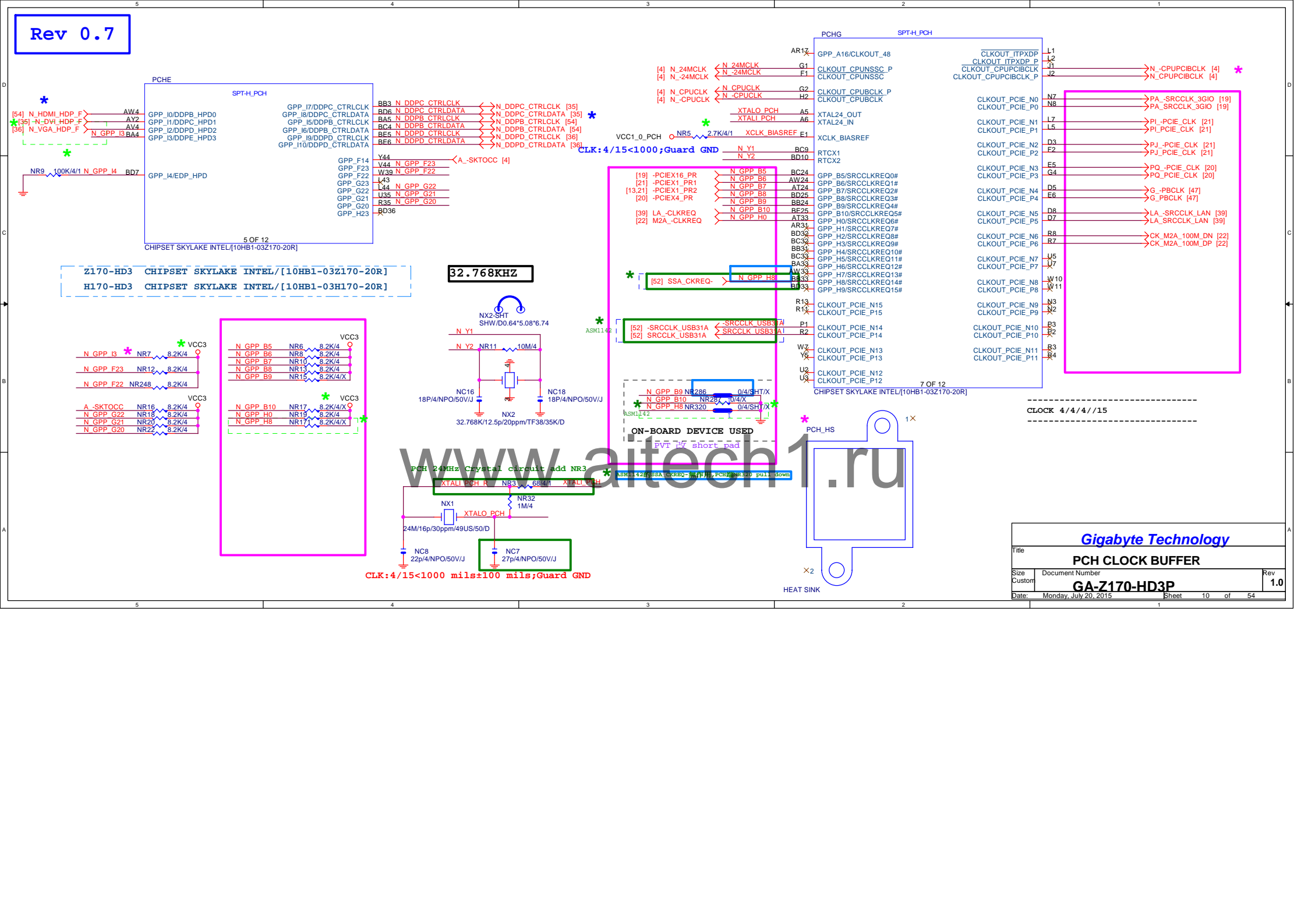
DDR12V Decouple

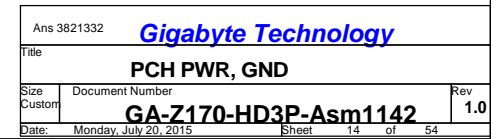


DDRVT Decouple



Rev 0.7



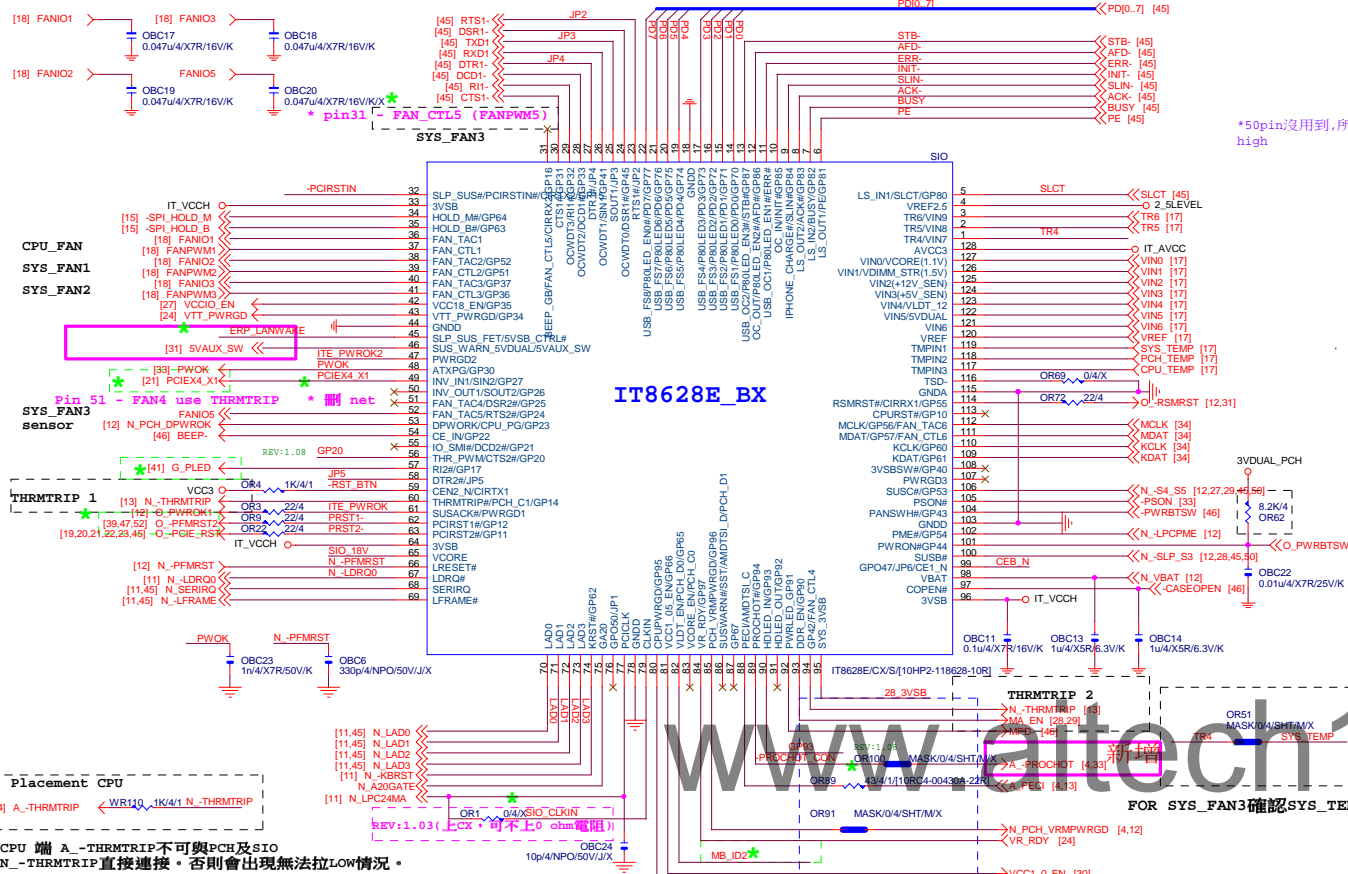


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Gigabyte Technology

Title		BIOS	
Size	Document Number	GA-Z170-HD3P	
Custom			Rev 1.0
Date:	Monday, July 20, 2015	Sheet	15 of 54

SIO IT8628CX REV:1.08



Placement CPU

CPU 端 A - THRMTRIP 不可與PCH及SIO N - THRMTRIP直接連接。否則會出現無法拉LOW情況。

Rev:1.08 (使用GP26時) - 漏Full High - 未使用可不接

Rev:1.08 (使用GP26時) - 漏Full High - 未使用可不接

Rev:1.08 (使用GP26時) - 漏Full High - 未使用可不接

Rev:1.08 (使用GP26時) - 漏Full High - 未使用可不接

Rev:1.08 (使用GP26時) - 漏Full High - 未使用可不接

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Rev:1.08 (使用GP26時) - 漏Full High - 未使用可不接

Rev:1.08 (使用GP26時) - 漏Full High - 未使用可不接

Rev:1.08 (使用GP26時) - 漏Full High - 未使用可不接

Rev:1.08 (使用GP26時) - 漏Full High - 未使用可不接

Rev:1.08 (使用GP26時) - 漏Full High - 未使用可不接

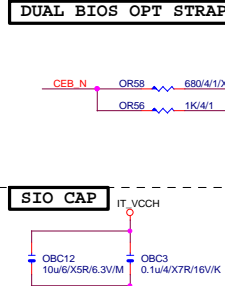
FAN TABLE

CPU_FAN	FAN_CTL1 FAN_TAC1
SYS_FAN1	FAN_CTL2 FAN_TAC2
SYS_FAN2	FAN_CTL3 FAN_TAC3
SYS_FAN3	FAN_CTL5 FAN_TAC5
OPT_FAN or SYS_FAN4	N/A
THRMTRIP1	YES PIN60
THRMTRIP2	YES PIN94

IT8620E GPIO問題匯整

PIN 50	GP26-第一次接上POWER時 會拉 LO
PIN 90/91	DEFAULT為HDLed FUNCTION, GP93 BYPASS TO GP92 高阻時 GP92 會被拉Lo (ITE BUG)
PIN 108	GP40--- POWER ON 時會拉 LO
PIN 111/112	MOUSE 跟FAN6 FUNCTION 擇一使用, 不然會互相干擾
PIN 22	PIN22+, 需高於3V+, 若低於 該部分COM PORT及LPT裝置 蜂鳴器會異常動作。

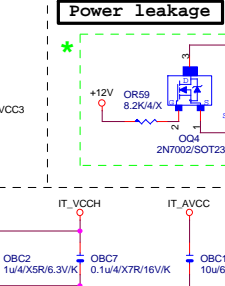
DUAL BIOS OPT STRAP



Power leakage



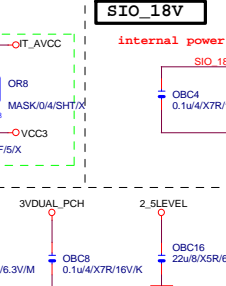
SIO 18V



SIO CAP



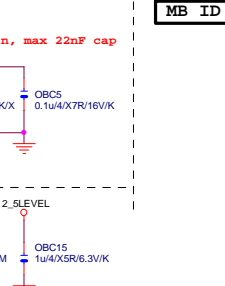
Power leakage



SIO 18V



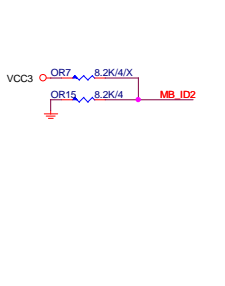
SIO CAP



Power leakage



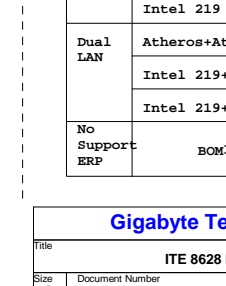
SIO 18V



SIO CAP



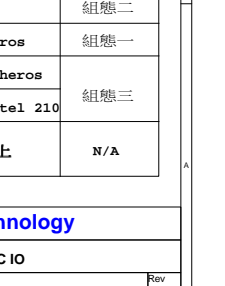
Power leakage



SIO 18V



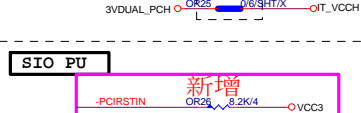
SIO CAP



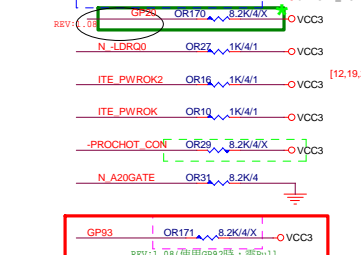
Power leakage



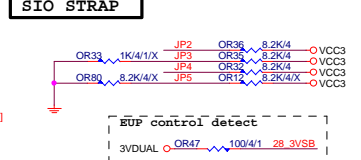
PWR SHT



SIO PU



SIO STRAP

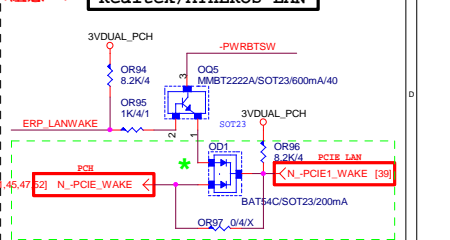


MB ID

JP2	1	Disable WDT
JP2	0	Enable WDT to rest PWROK
JP3	1	Dual BIOS CS PIN Disable
JP3	0	Dual BIOS CS PIN Enable
JP4	0	k8 power sequence function is Disable
JP4	1	k8 power sequence function is Enable
JP5	1	anti-surge Disable
JP5	0	anti-surge Enable
JP3	1 1	The default value of EC Index 63h/6Bh/73h is 80h.
JP3	1 0	The default value of EC Index 63h/6Bh/73h is FFh.
JP5	0 1	The default value of EC Index 63h/6Bh/73h is 00h.
JP5	0 0	The default value of EC Index 63h/6Bh/73h is 40h.

ERP WAKE on LAN (依LAN組態選擇)

(組態一) Realtek/ATHEROS LAN



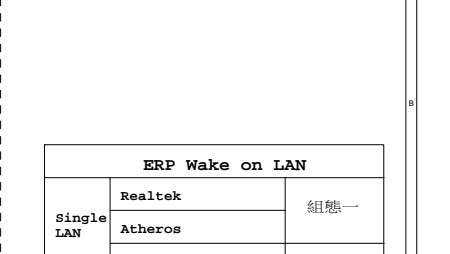
ERP WAKE on LAN (依LAN組態選擇)

(組態二) Realtek/ATHEROS LAN



ERP WAKE on LAN (依LAN組態選擇)

(組態三) Realtek/ATHEROS LAN



ERP WAKE on LAN (依LAN組態選擇)

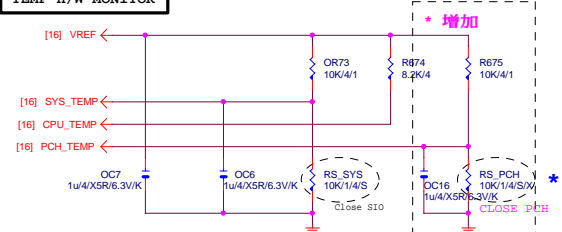
(組態四) Realtek/ATHEROS LAN

ERP Wake on LAN		
Single LAN	Realtek	組態一
	Atheros	組態二
Dual LAN	Intel 219	組態一
	Atheros+Atheros	組態二
No Support ERP	Intel 219+Intel 210	組態三
	BOM不上	N/A

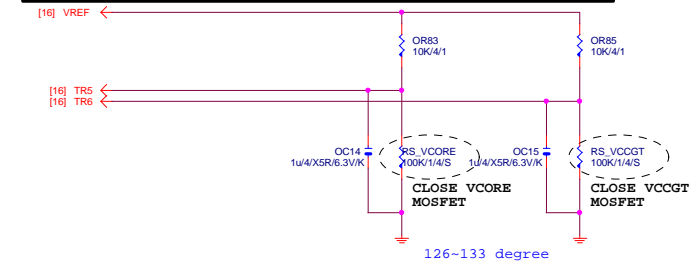
Gigabyte Technology

Title			ITE 8628 LPC IO		
Size			Document Number		
Custom			GA-Z170-HD3P		
Date:			Monday, July 20, 2015		
Sheet			16 of 54		
Rev			1.0		

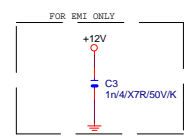
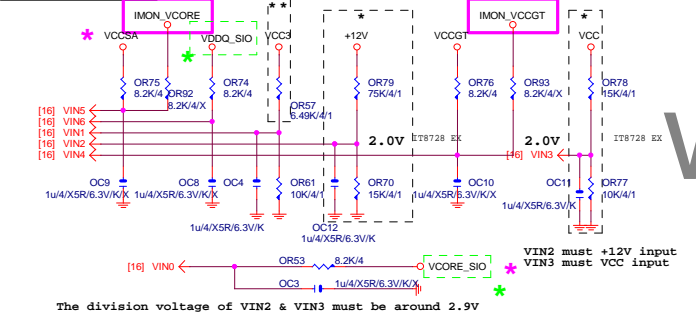
TEMP H/W MONITOR

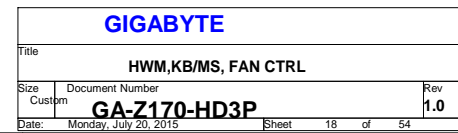
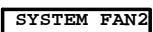
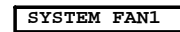


RS_VCORE, RS_VCCGT, CLOSE CPU_VCORE & VCCGT MOSFET

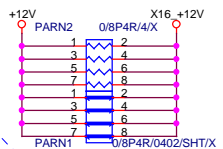


VOLTAGE-- H/W MONITOR





Rev 0.1

* +12 protect
short-wire test

[8,9,12,20,21,24,32,48] N_SMBCLK
[8,9,12,20,21,24,32,48] N_SMBDATA
[12,16,20,21,45,47,52] N_-PCIE_WAKE

PA_EXP_RXP0_15] >> PA_EXP_RXP0[0..15] [4]
PA_EXP_RXN0_15] >> PA_EXP_RXN0[0..15] [4]
PA_EXP_TXP0_15] >> PA_EXP_TXP0[0..15] [4]
PA_EXP_TXN0_15] >> PA_EXP_TXN0[0..15] [4]

PA_EXP_TXP0	PAC5	0.22u4/X5R/6.3V/K	PA_EXP_TXP0 C
PA_EXP_TXN0	PAC4	0.22u4/X5R/6.3V/K	PA_EXP_TXN0 C
PA_EXP_TXP1	PAC6	0.22u4/X5R/6.3V/K	PA_EXP_TXP1 C
PA_EXP_TXN1	PAC7	0.22u4/X5R/6.3V/K	PA_EXP_TXN1 C
PA_EXP_TXP2	PAC8	0.22u4/X5R/6.3V/K	PA_EXP_TXP2 C
PA_EXP_TXN2	PAC9	0.22u4/X5R/6.3V/K	PA_EXP_TXN2 C
PA_EXP_TXP3	PAC10	0.22u4/X5R/6.3V/K	PA_EXP_TXP3 C
PA_EXP_TXN3	PAC11	0.22u4/X5R/6.3V/K	PA_EXP_TXN3 C
PA_EXP_TXP4	PAC12	0.22u4/X5R/6.3V/K	PA_EXP_TXP4 C
PA_EXP_TXN4	PAC13	0.22u4/X5R/6.3V/K	PA_EXP_TXN4 C
PA_EXP_TXP5	PAC14	0.22u4/X5R/6.3V/K	PA_EXP_TXP5 C
PA_EXP_TXN5	PAC15	0.22u4/X5R/6.3V/K	PA_EXP_TXN5 C
PA_EXP_TXP6	PAC16	0.22u4/X5R/6.3V/K	PA_EXP_TXP6 C
PA_EXP_TXN6	PAC17	0.22u4/X5R/6.3V/K	PA_EXP_TXN6 C
PA_EXP_TXP7	PAC18	0.22u4/X5R/6.3V/K	PA_EXP_TXP7 C
PA_EXP_TXN7	PAC19	0.22u4/X5R/6.3V/K	PA_EXP_TXN7 C
PA_EXP_TXP8	PAC21	0.22u4/X5R/6.3V/K	PA_EXP_TXP8 C
PA_EXP_TXN8	PAC20	0.22u4/X5R/6.3V/K	PA_EXP_TXN8 C
PA_EXP_TXP9	PAC22	0.22u4/X5R/6.3V/K	PA_EXP_TXP9 C
PA_EXP_TXN9	PAC23	0.22u4/X5R/6.3V/K	PA_EXP_TXN9 C
PA_EXP_TXP10	PAC24	0.22u4/X5R/6.3V/K	PA_EXP_TXP10 C
PA_EXP_TXN10	PAC25	0.22u4/X5R/6.3V/K	PA_EXP_TXN10 C
PA_EXP_TXP11	PAC26	0.22u4/X5R/6.3V/K	PA_EXP_TXP11 C
PA_EXP_TXN11	PAC27	0.22u4/X5R/6.3V/K	PA_EXP_TXN11 C
PA_EXP_TXP12	PAC28	0.22u4/X5R/6.3V/K	PA_EXP_TXP12 C
PA_EXP_TXN12	PAC29	0.22u4/X5R/6.3V/K	PA_EXP_TXN12 C
PA_EXP_TXP13	PAC30	0.22u4/X5R/6.3V/K	PA_EXP_TXP13 C
PA_EXP_TXN13	PAC31	0.22u4/X5R/6.3V/K	PA_EXP_TXN13 C
PA_EXP_TXP14	PAC32	0.22u4/X5R/6.3V/K	PA_EXP_TXP14 C
PA_EXP_TXN14	PAC33	0.22u4/X5R/6.3V/K	PA_EXP_TXN14 C
PA_EXP_TXP15	PAC34	0.22u4/X5R/6.3V/K	PA_EXP_TXP15 C
PA_EXP_TXN15	PAC35	0.22u4/X5R/6.3V/K	PA_EXP_TXN15 C

PCIEX16:16/5/5/5/16

PCI-E REV:1.1--> 2.5GHZ

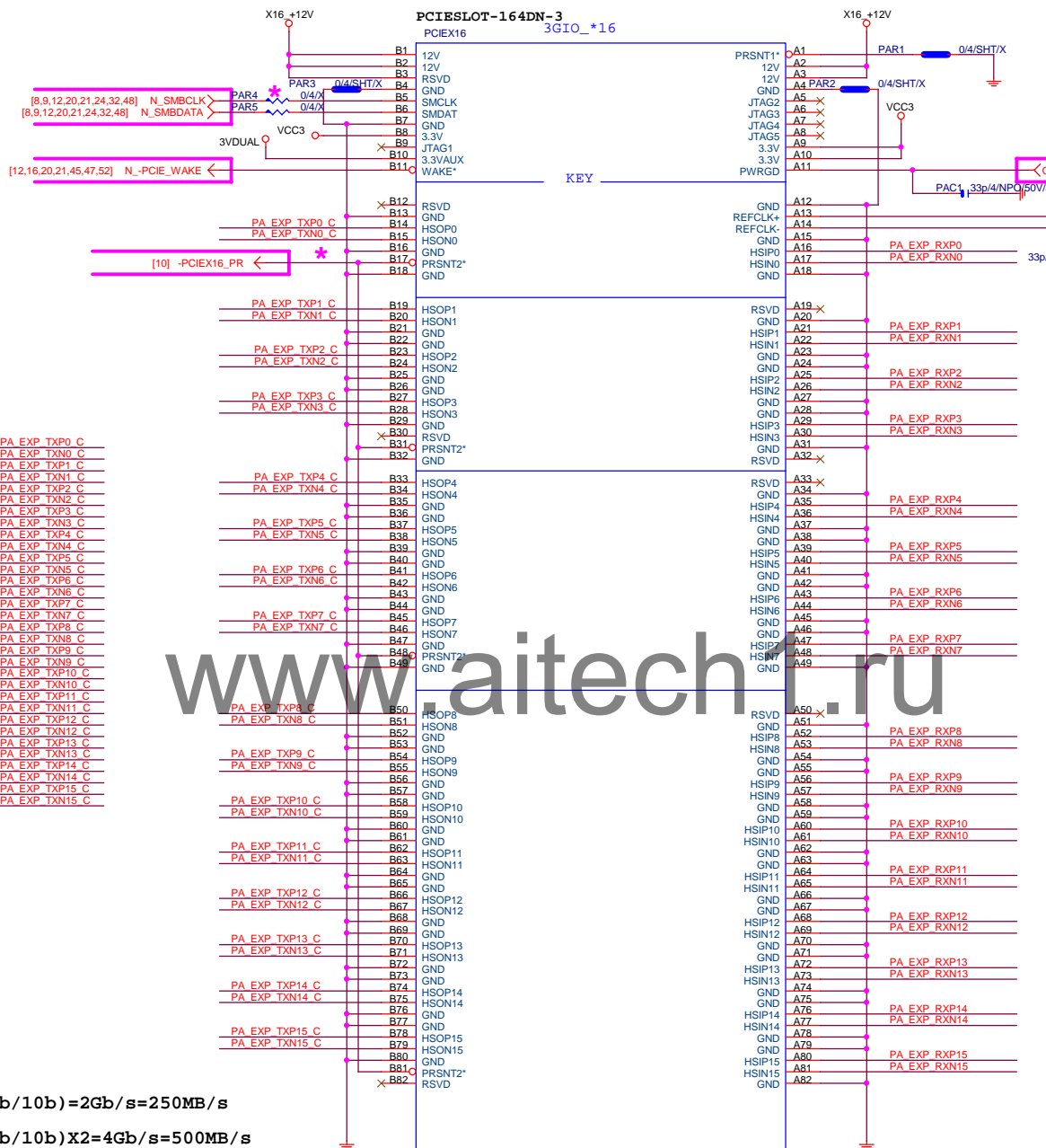
PCE-E X1(單向) BANDWIDTH=2.5GHz*(8b/10b)=2Gb/s=250MB/s

PCE-E X1(雙向) BANDWIDTH=2.5GHz*(8b/10b)X2=4Gb/s=500MB/s

PCE-E X16(單向) BANDWIDTH=2.5GHz*(8b/10b)X16=32Gb/s=4GB/s

PCE-E X16(雙向) BANDWIDTH=2.5GHz*(8b/10b)X16X2=64Gb/s=8GB/s

PCI-E REV:2.0--> 5GHZ



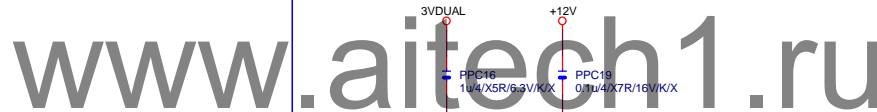
* PCI-E/16X-164P/GYL/ONG DOUBLE/HK*2

PCIEX16需更新無強化孔的Footprint

一般Footprint :PCIESLOT-164P

Gigabyte Technology			
Title			
PCI EXPRESS * 16			
Size	Document Number	Rev	
Custom	GA-Z170-HD3P	1.0	
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PCIE*4



要改66PIN

PCIEX1_3

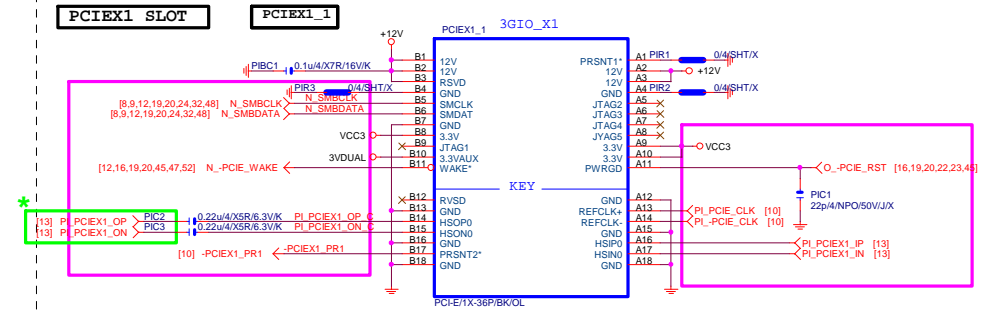
PPR11 PU VCC3, PCH端的-PCIEX1_PR2已經預留NR10
[10,13] N_GPP_G3

PPD2

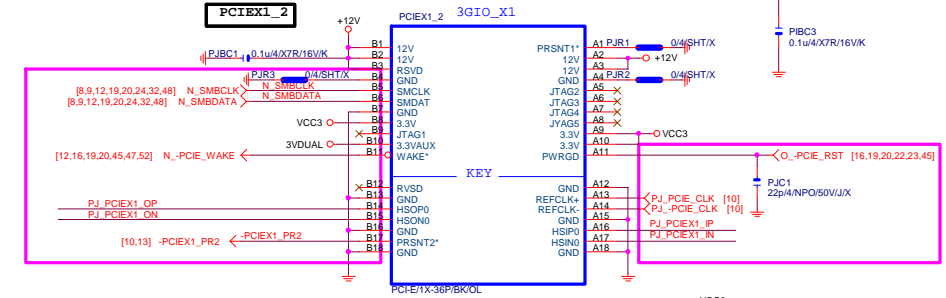
PPU2

	N_GPP_G3 (PCH GPP_G3)	PCIEX4_X1 (SIO_GPIO27)
PCIEX4 -> X4 M2_WIFI -> N/A PCIEX1 -> N/A (Default)	H	H
PCIEX4 -> X1 M2_WIFI -> X1 PCIEX1 -> X1	L	L

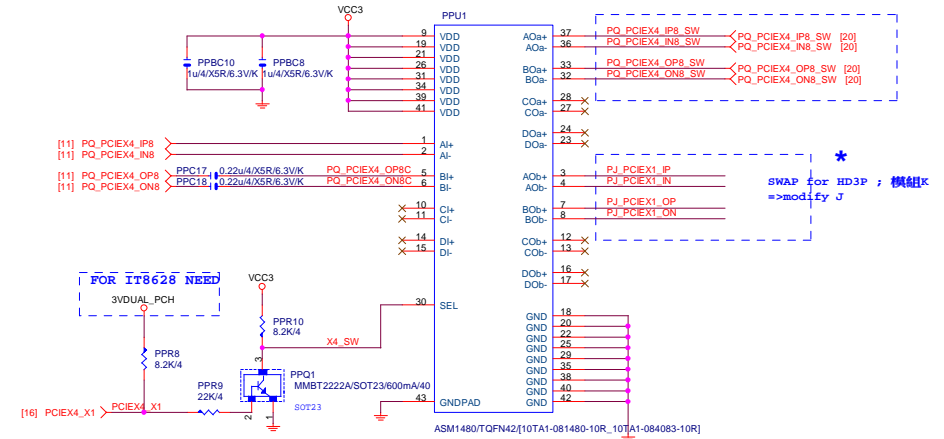
PCIEX1 SLOT



PCIEX1_2



PCIEX4/X1 SWITCH



Function	SEL
XI--> x0h	L;PCIEX4 SLOT-->X1
XI--> x0h	H;PCIEX4 SLOT-->X1

M.2 Lane4 from PCH port18

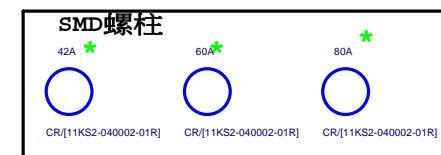
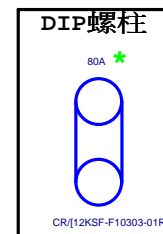
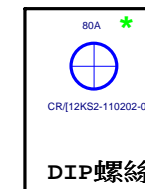
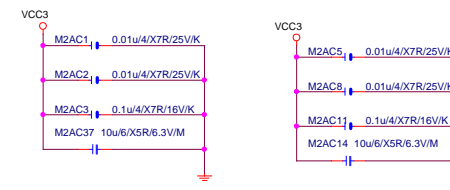
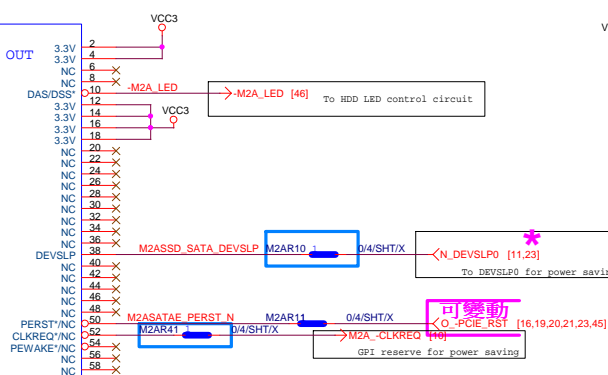
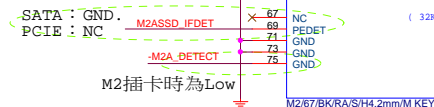
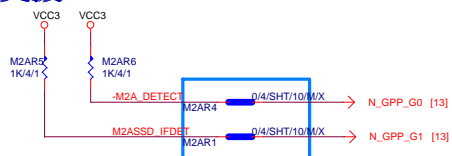
M.2 Lane3 from PCH port17

M.2 Lane2 from PCH port16

M.2 Lane2 from PCH port15

需與M2_-CLKREQ對應

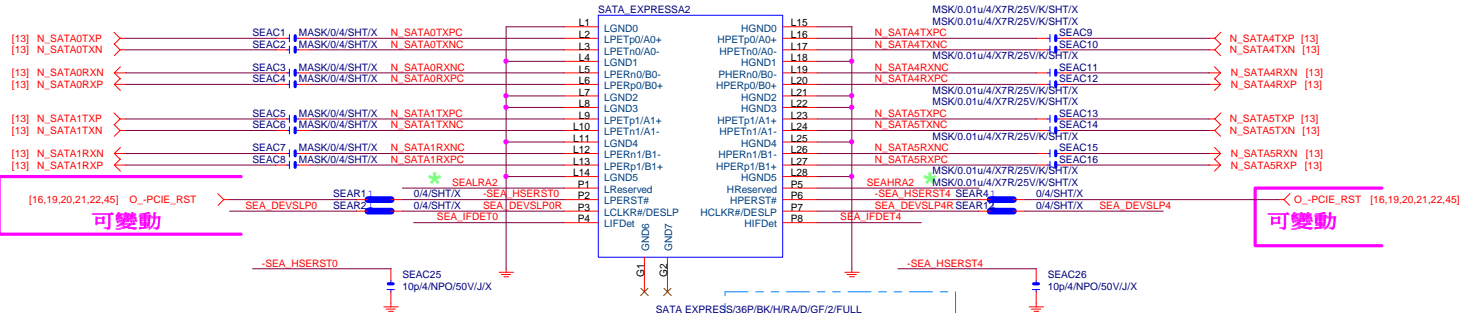
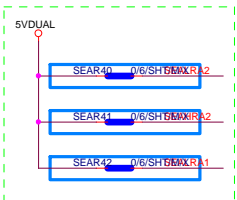
支援SATA and M.2 function



M.2 有插卡 /沒插卡 GPP_G0	M.2插何種卡? GPP_G1	SATA Express 插何種硬碟? GPP_E0/E2/F1	IO15 (S0)	IO16 (S1)	IO17	IO18	IO19 (S0)	IP20 (S1)
有插卡 (Low)	SATA Mode (Low)	SATA (Hi)	SATA (M.2)	PCIE x1	PCIE x1	PCIE x1	PCIE x1	SATA
		SATA Express (Low)	SATA (M.2)	PCIE x1	PCIE x1	PCIE x1	SATA Express	
	PCIE Mode (Hi)	SATA (Hi)	PCIE x4 (For M.2)				SATA	SATA
		SATA Express (Low)	PCIE x4 (For M.2)				SATA Express	
沒插卡 (Hi)	Don't Care (Hi)	SATA (Hi)	PCIE x4				SATA	SATA
		SATA Express (Low)	PCIE x4				SATA Express	

SATA EXPRESS 下層 To SATA3
port0/1

SATA EXPRESS 上層 To SATA3
port4/5



* 單層+2SATA
Z170-HD3 :36P ,SATA EXPRESS/36P/BK/H/RA/D/GF/2/FULL
H170-HD3 :32P ,SATA EXPRESS/32P/BK/H/RA/D/GF/2

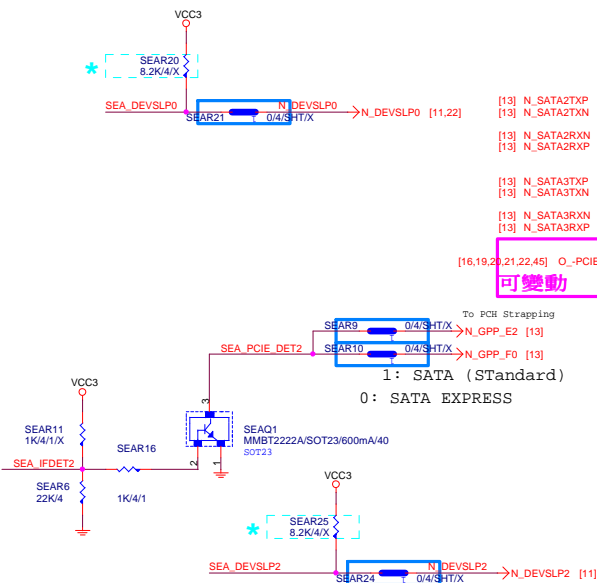
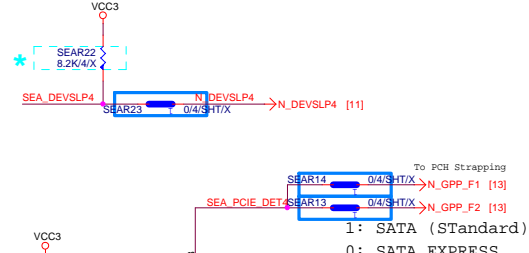
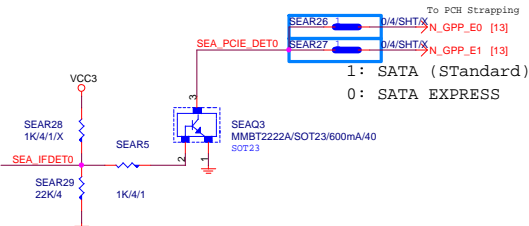
SATA EXPRESS料號

雙層:11NR6-C10236-11R

單層+2SATA : 11NR6-C10232-11F

單層:11NR6-C10118-31R

To SATA3
port2/3



SATA 5 (文字面寫SATA 1)
SATA 4 (文字面寫SATA 0)
SATA 3
SATA 2
SATA 1 (文字面寫SATA 5)
SATA 0 (文字面寫SATA 4)

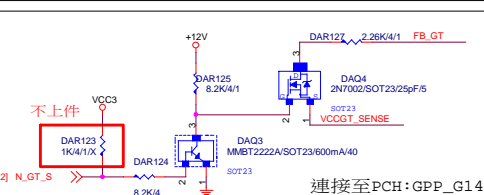
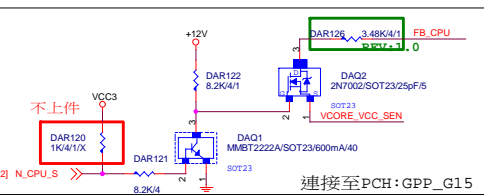
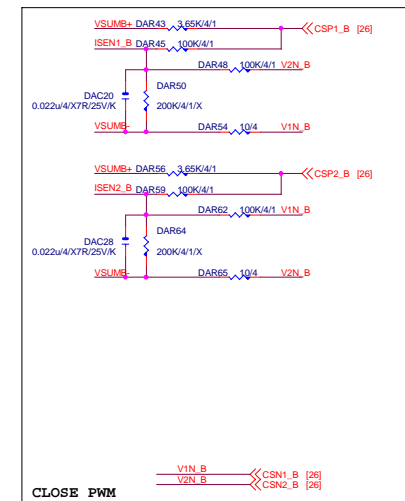
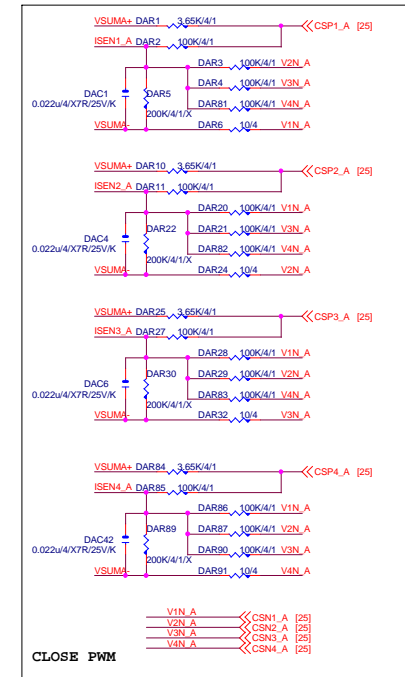
Gigabyte Technology

SATA EXPRESS

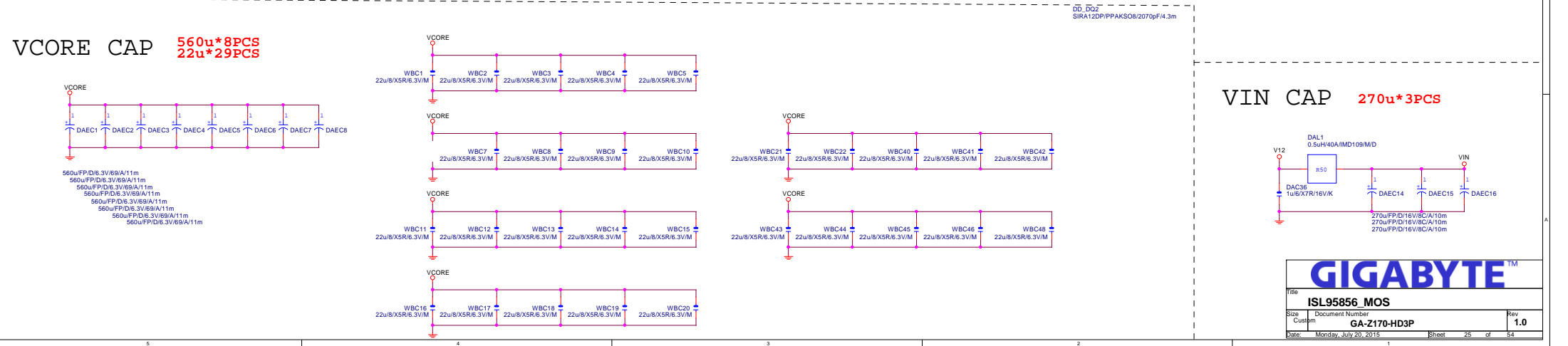
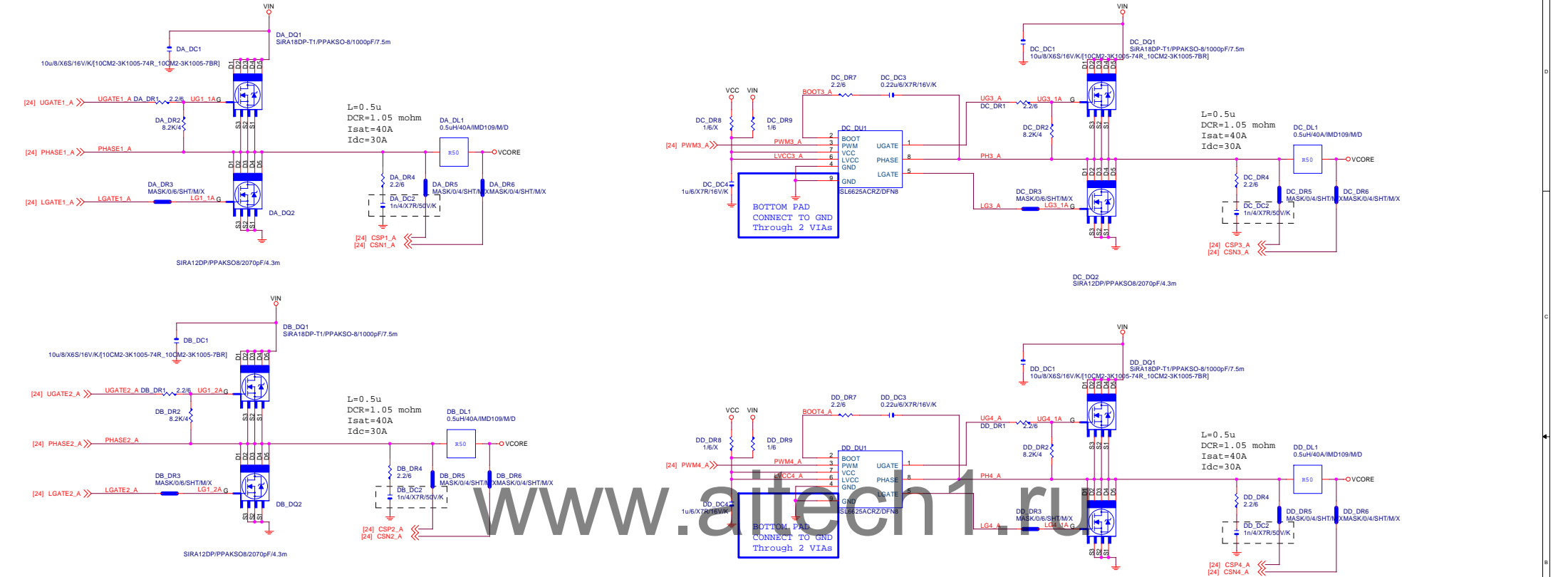
GA-Z170-HD3

1.

Title			
SATA EXPRESS			
Size	Document Number		Rev
Custom	GA-Z170-HD3P		
Date:	Monday, July 20, 2015	Sheet	23 of 54

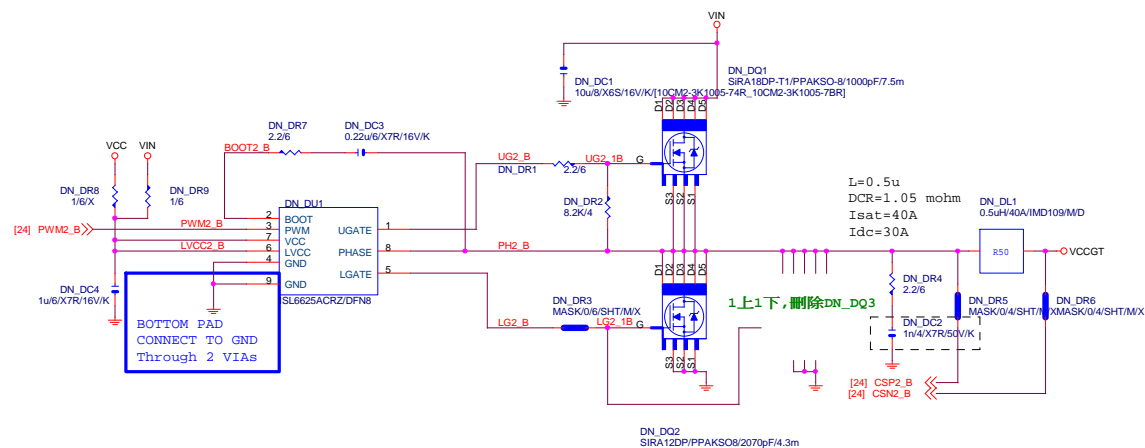
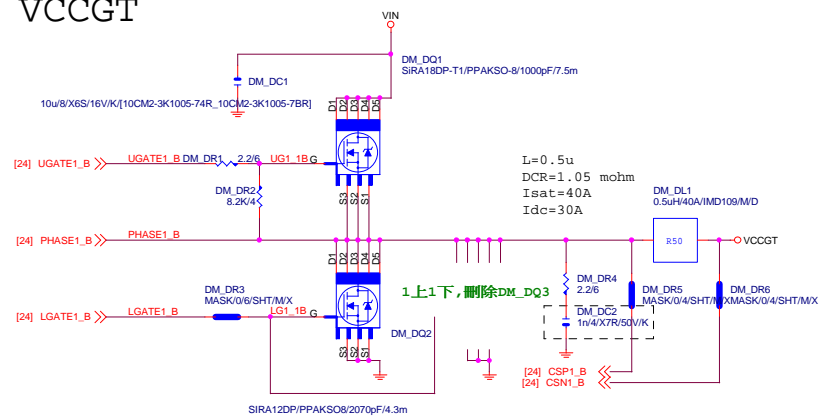


VCORE

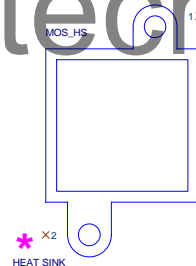
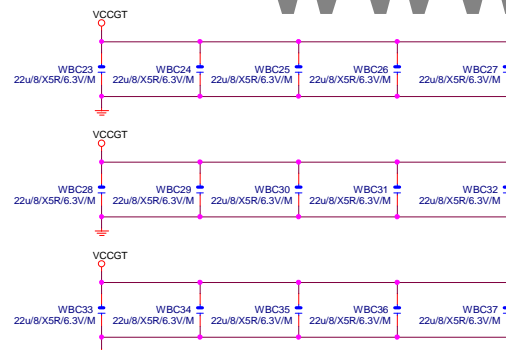
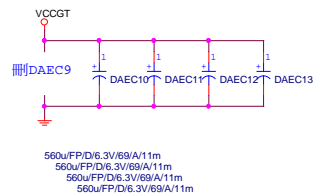


ISL95856 MOS		
Size	Document Number	Rev
Custom	GA-2170-HD3P	1.0
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VCCGT



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VCCGT CAP 560u*5PCS
22u*15PCSfootprint :
MOSHHSINK-Z1704-HD3

GIGABYTE™			
Title			
ISL95856 MOS			
Size	Document Number	Rev	
Custom	GA-Z170-HD3P	1.0	
Date:	Monday, July 20, 2015	Sheet	26 of 54

DDR4



$L = 0.5 \mu$
 $DCR = 1.05 \text{ mohm}$
 $I_{sat} = 40A$
 $I_{dc} = 30A$

Remote sense請從最重的負載端點拉回

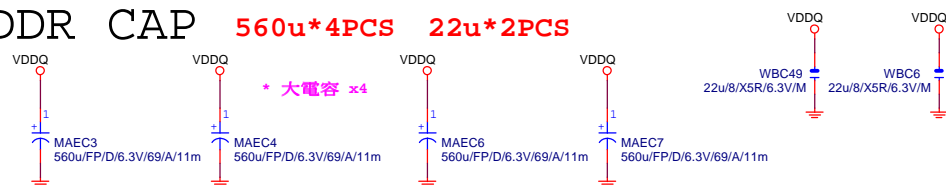


For PVT : for chang Mode=>
MAR110/MAR111不能改short pad

DDR_VTT_CTL	MAR110	0/4	DDRVTT_EN
N -SLP_S3	MAR111	0/4	DDRVTT_BOOT

MAU1上NCT3103S時上件

DDR CAP 560u*4PCS 22u*2PCS



DDRVTT CAP

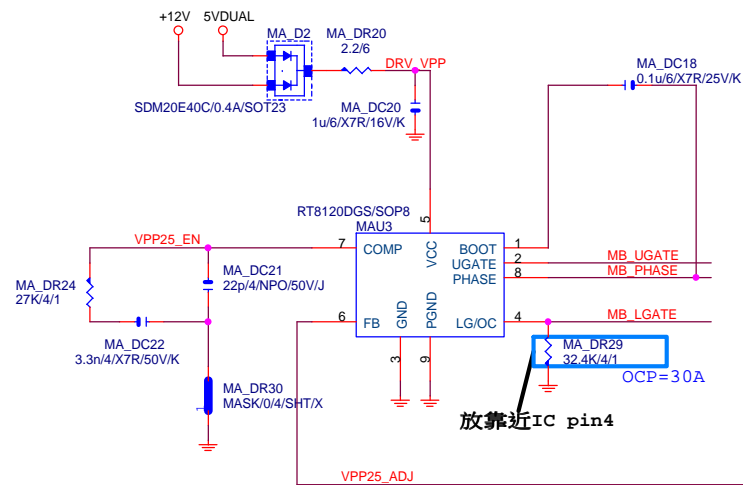
**GIGABYTE™**

RT8120 DDR4 POWER

Size	Document Number	Rev
Custom	GA-Z170-HD3P	1.0
Date:	Monday, July 20, 2015	Sheet 28 of 54

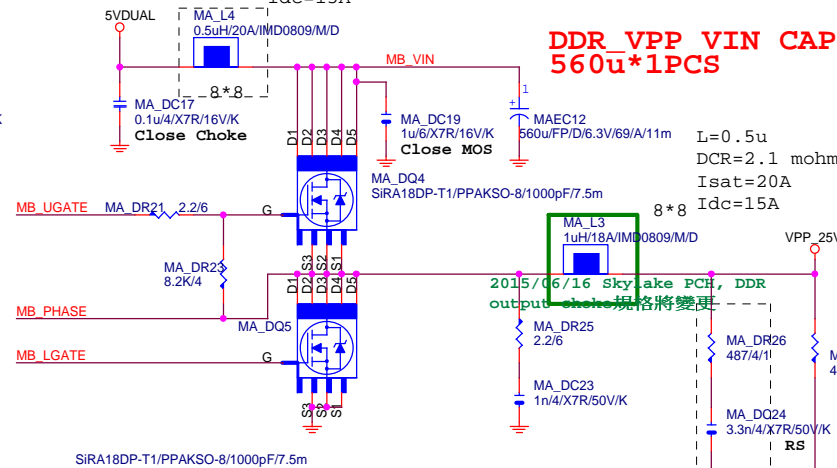
REV:0.88

VPP_25V



L=0.5u
DCR=2.1 mohm
Isat=20A
Idc=15A

CHOKE與CAP料號可變

DDR_VPP VIN CAP
560u*1PCS

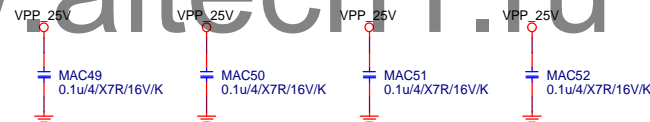
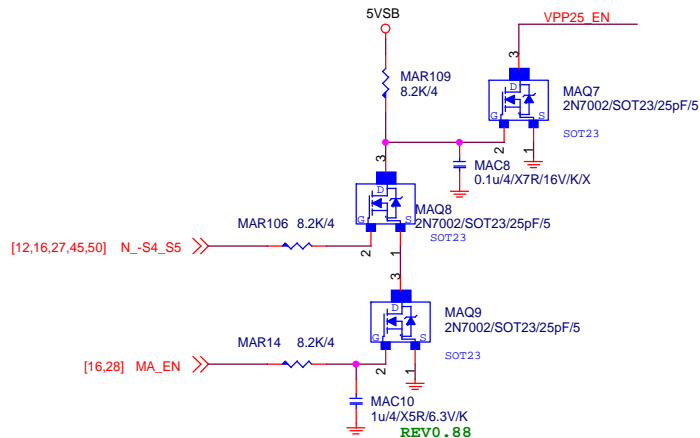
SUPPORT DDR4 2.5V

Remote sense請從最重的負載端點拉回

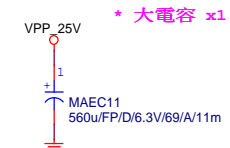
www.aitech1.ru

PWR_SEQ

* 刪 MA_DR32



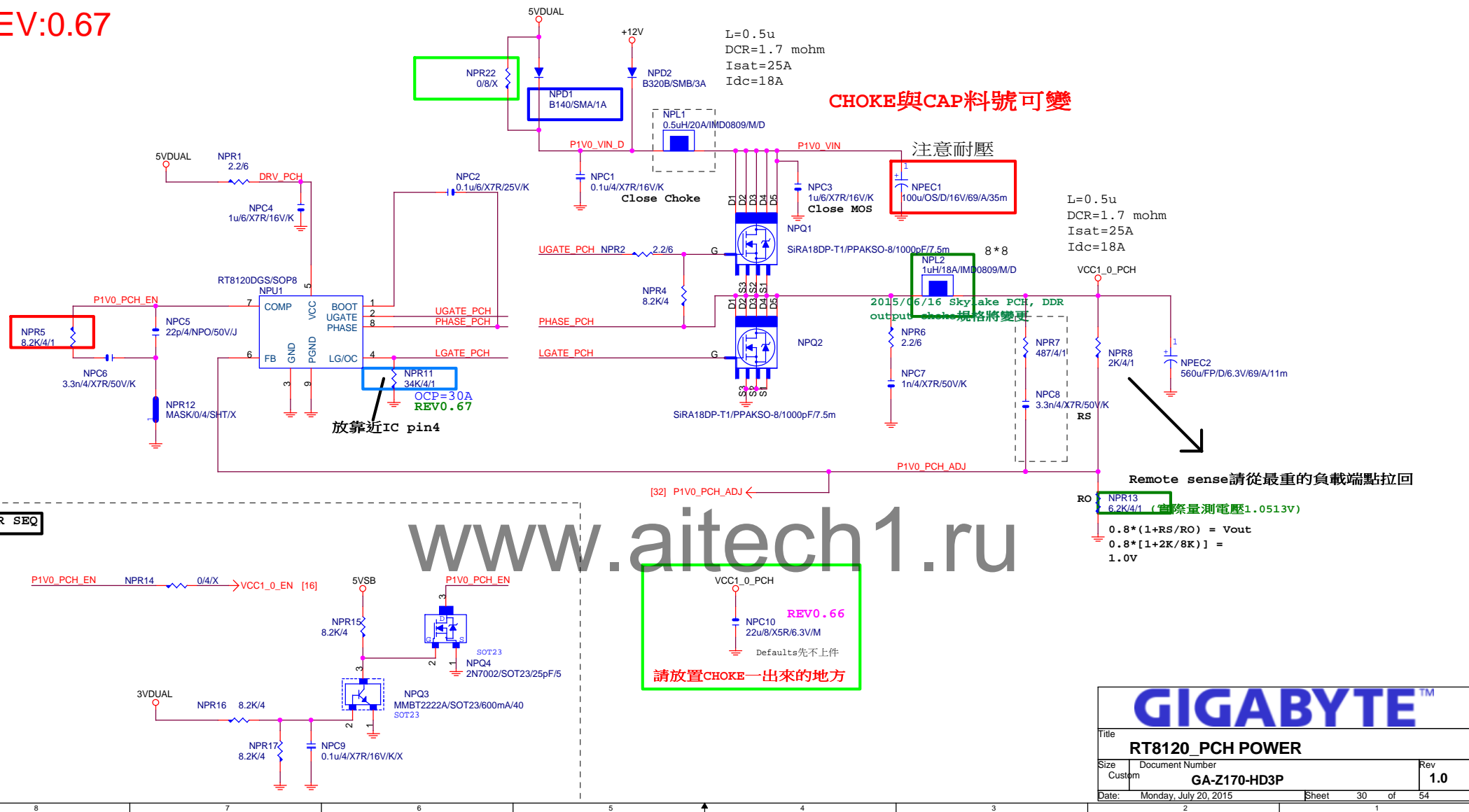
VPP CAP 560u*1PCS



GIGABYTE™

Title		
RT8120_VPP25 POWER		
Size	Document Number	Rev
Custom	GA-Z170-HD3P	1.0
Date:	Monday, July 20, 2015	Sheet 29 of 54

REV:0.67



CHOKES與CAP料號可變

注意耐壓

放靠近IC pin4

Remote sense請從最重的負載端點拉回

RO NPR13 6.2K/4/1 (實際量測電壓1.0513V)
 $0.8 * (1 + RS / RO) = V_{out}$
 $0.8 * [1 + 2K / 8K] = 1.0V$

請放置CHOKES—出來的地方

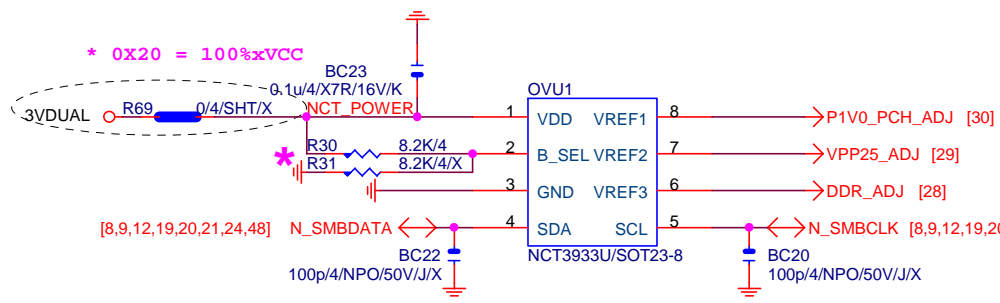
GIGABYTE™			
Title			
RT8120_PCH POWER			
Size	Document Number	Rev	
Custom	GA-Z170-HD3P	1.0	
Date:	Monday, July 20, 2015	Sheet	30 of 54

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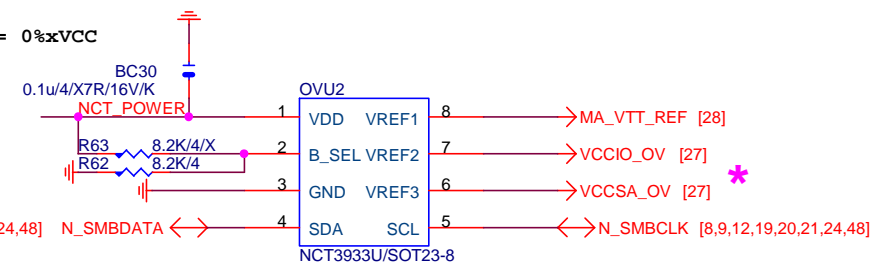
Gigabyte Technology

Title			
DISCRETE POWER			
Size	Document Number	Rev	
Custom	GA-Z170-HD3P	1.0	
Date:	Monday, July 20, 2015	Sheet	31 of 54

OVER VOLTAGE



0X2A = 0%xVCC



0X22 = 75%xVCC

* 删除 OVU3

NCT3933	0X2A	0X20	0X22
VREF1	DDRVTT	VREF_DDRA_DQ	PCH Core
VREF2	VREF_DDRA_CA	N/A	VCC1_5_PCH
VREF3	VREF_DDRA_CA	VREF_DDRB_DQ	SMREF

Gigabyte Technology

Title: CPU CORE VR-2

Size: Custom

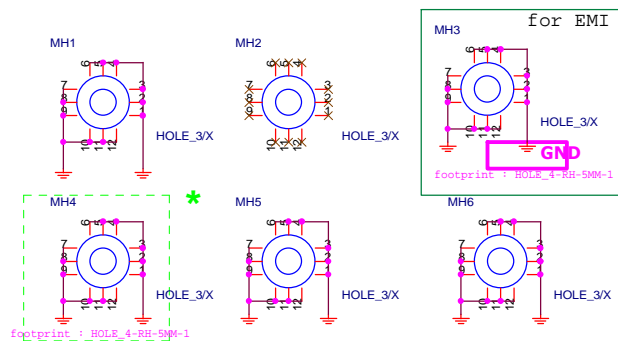
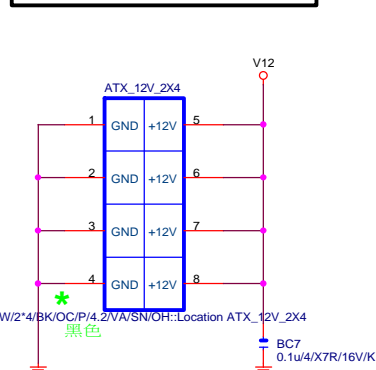
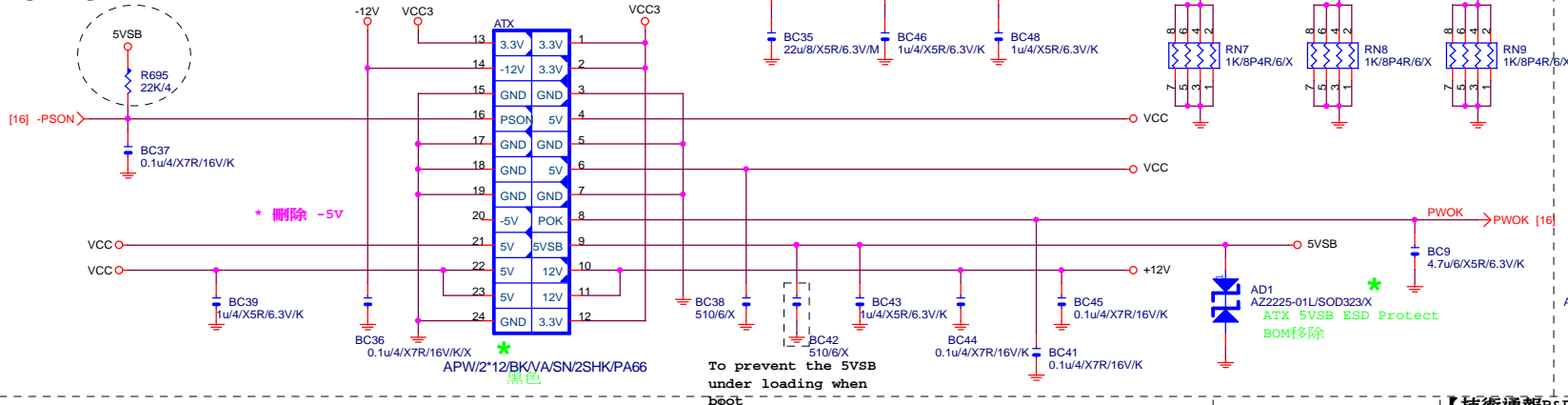
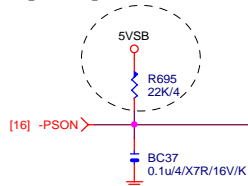
Document Number: GA-Z170-HD3P

Date: Monday, July 20, 2015

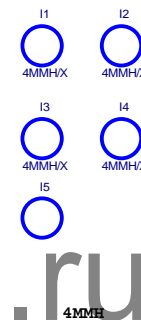
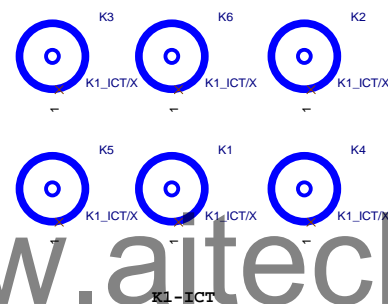
Sheet 32 of 54

Rev 1.0

ATXX4 POWER CONNECTOR

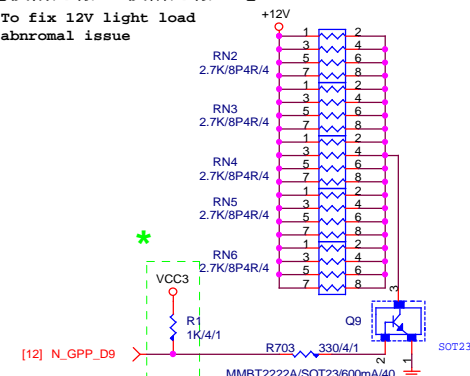


有TYPE-C螺絲洞改半圈, footprint : HOLE_4-RH-5MM-1



【技術通報R&D技術通報153】

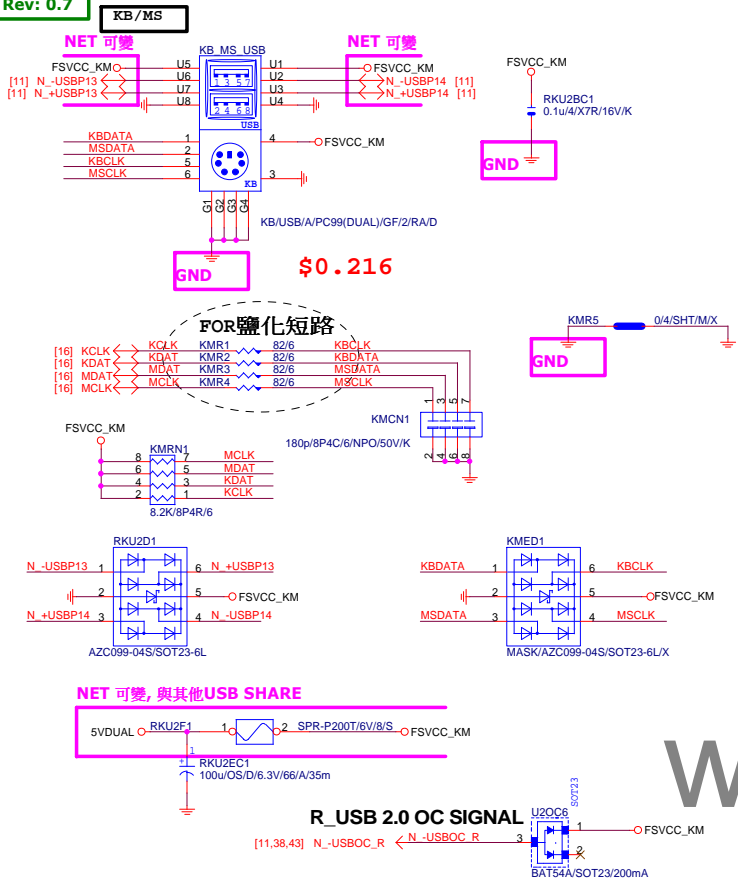
To fix 12V light load
abnromal issue



-PROHOT

COUPON



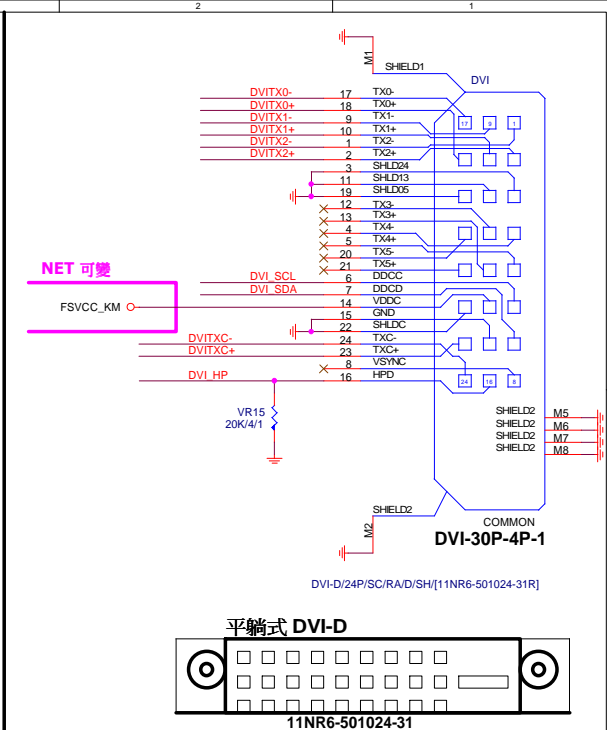


USB_DAC

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Gigabyte Technology

Title				AUDIO JACK	
Size				GA-Z170-HD3P	
Date:				Monday, July 20, 2015	Sheet 34 of 54



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省X'TAL COST DOWN:

1. 上件:

DVC28 [10p/4/NPO/50V/J]

DVC11 [10p/4/NPO/50V/J]~修改值

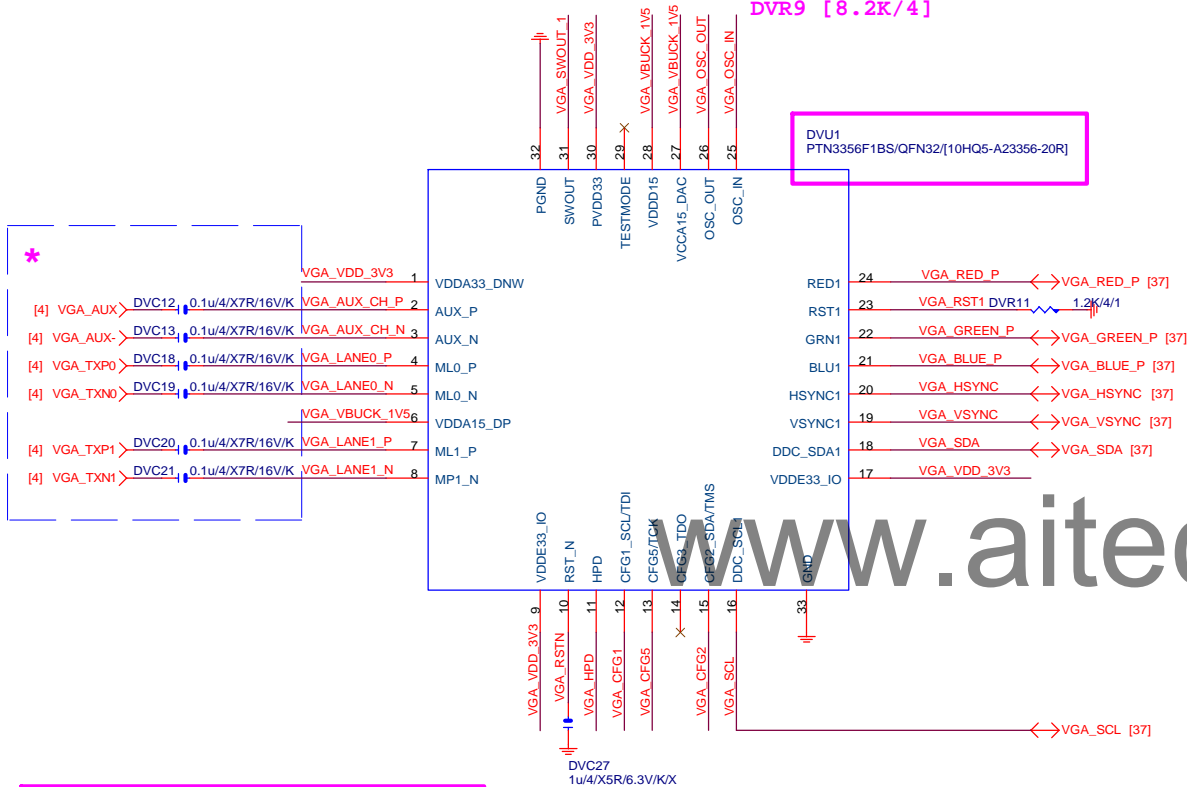
DVR10 [8.2K/4]

2. 删除:

DVX1 [25M/16p/30ppm/49US/20/D]

DVC10 [20p/4/NPO/50V/J]

DVR9 [8.2K/4]



放置PCH端



Timing diagram for the VGA signal. The signal is shown as a red line with a ground symbol at the start. It has two transitions: one labeled 'DVR9 8.2K/4' and another labeled 'DVR10 8.2K/4/X'. The signal is labeled 'VGA_CFG5' and 'VGA_VDD_3V3'. The timing values are: LO: 25M, OPEN: 27M, and HI: 24M.

VCC3

DVL1
0/6/SHT/M/X

VGA_VDD_3V3

DVC14
4.7uF/6/X5R/6.3V/K

DVC15
0.1uF/4/X7R/16V/K

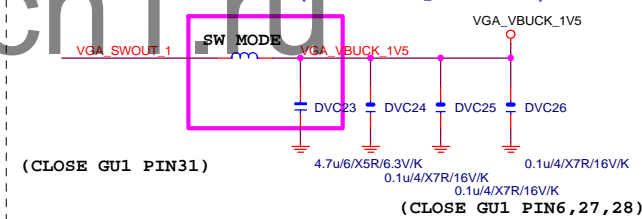
DVC16
0.1uF/4/X7R/16V/K

DVC17
0.1uF/4/X7R/16V/K

DVC22
0.1uF/4/X7R/16V/K

(CLOSE GU1 PIN1,9,17,30)

```
LDO  MODE:DVL2,DVC23-->X
S.W  MODE:DVL2,DVC23-->O
```



Non-Compliant

DVR12
8.2K/4

VGA_CFG1

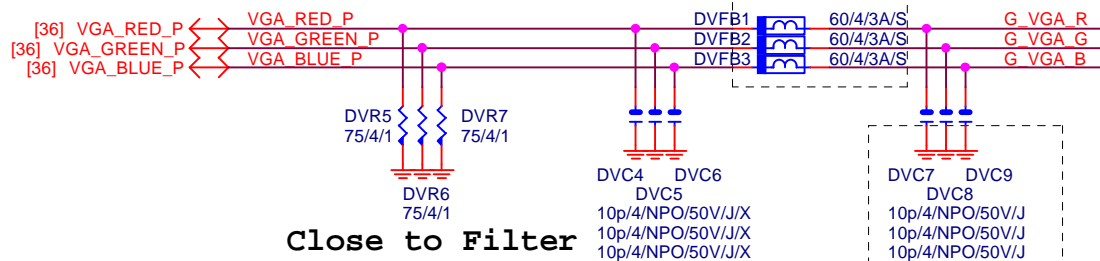
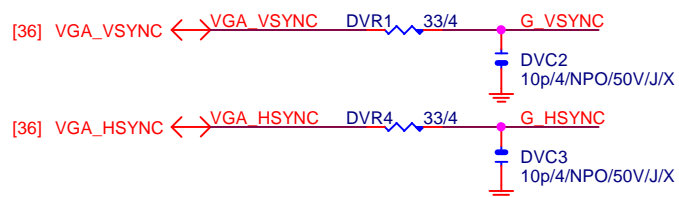
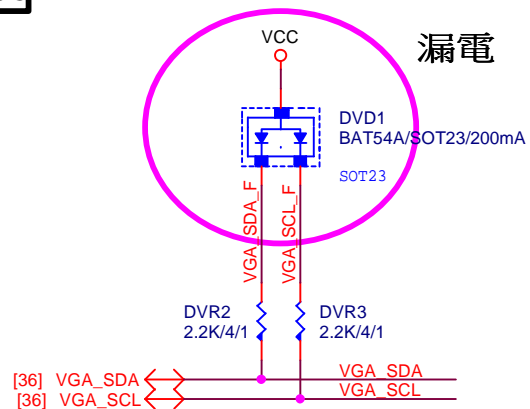
DVR13
8.2K/4/X

VGA_VDD_3V3

VGA_CFG2

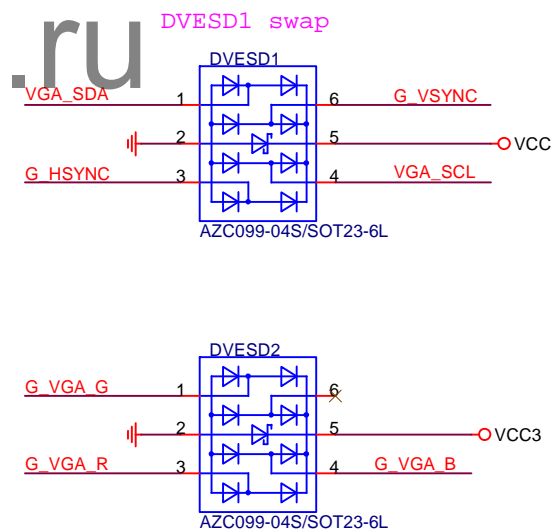
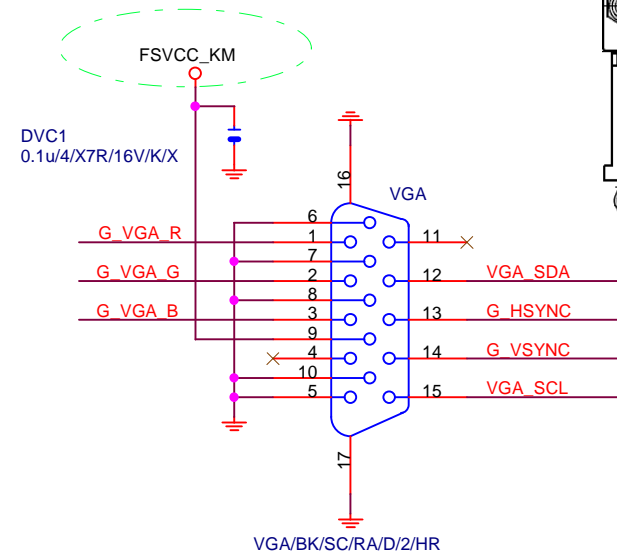
DVR14
8.2K/4

VGA_VDD_3V3



Close to Filter

FOR EMI



Gigabyte Technology
NXP-PTN3356

Size Custom Document Number GA-Z170-HD3P

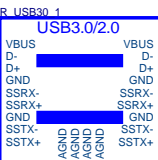
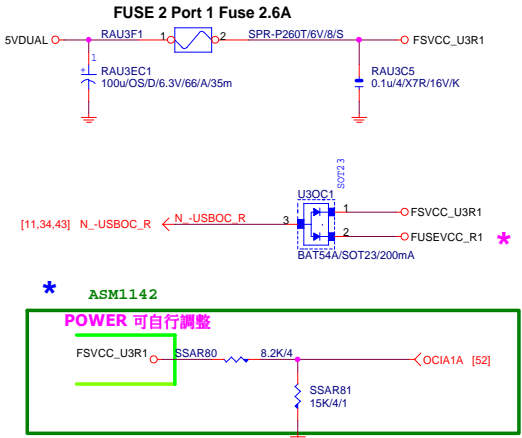
Rev 1.0

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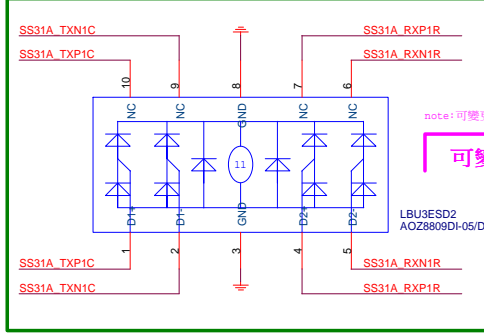
Rev: 0.7

* USB 電容前後NET 可自行調整

R_USB30_1

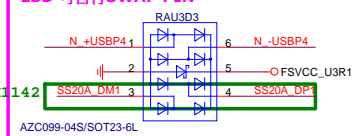


USB 電容前後NET 可自行調整



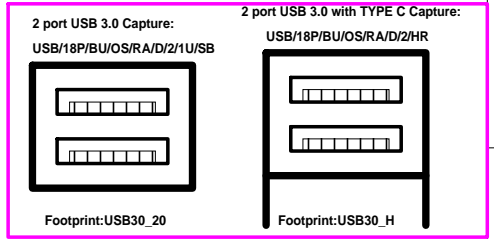
ASM1142

ESD 可自行SWAP PIN



ASM1142

CONNECTOR 自行調整

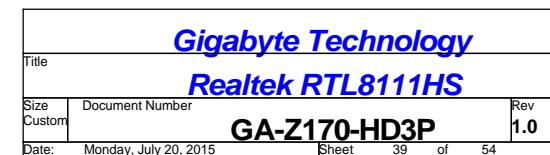


ASM1142 USB31 Host Rev0.62

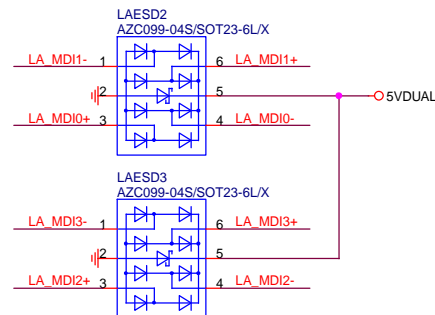
R_USB30_2

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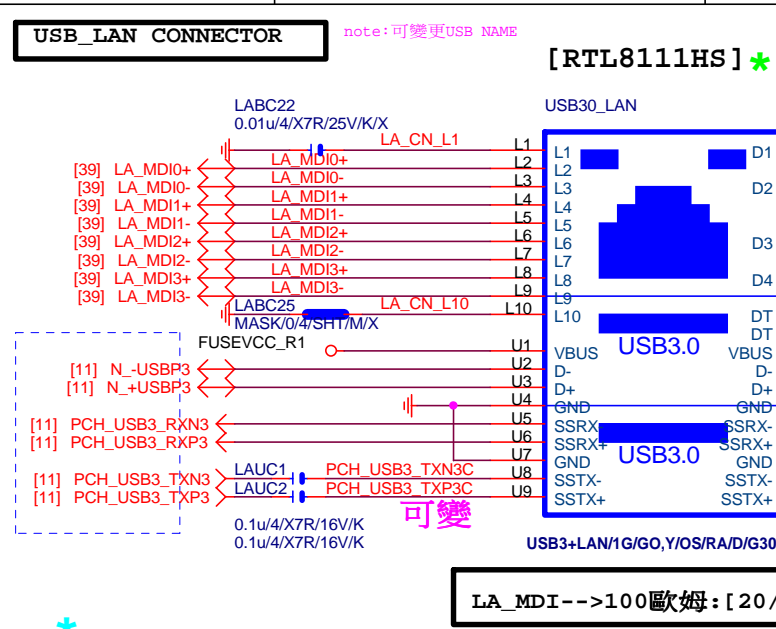
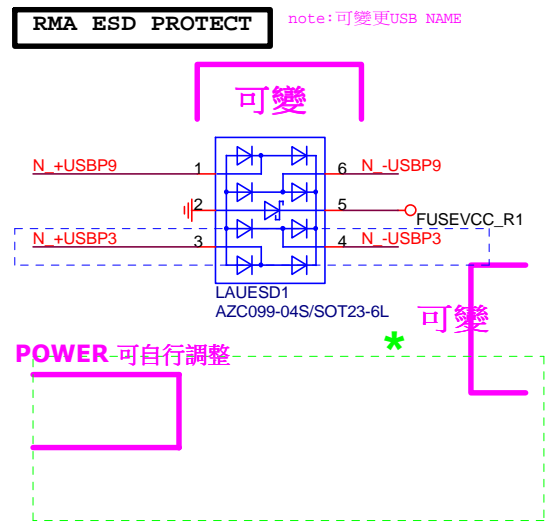
KB_MS_USB3



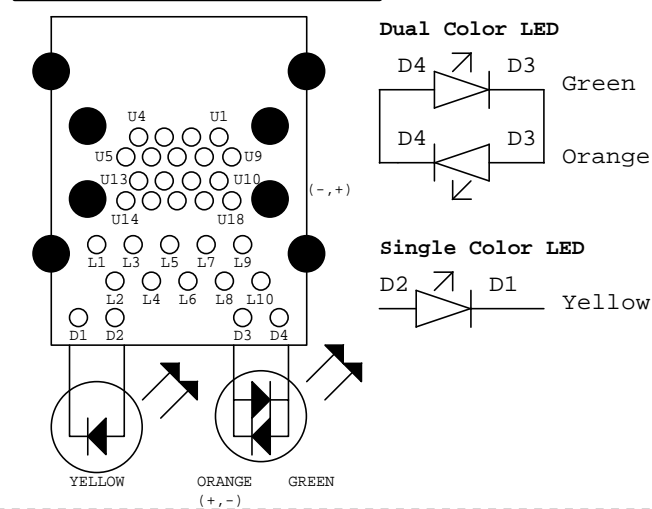
MDI ESD預留*



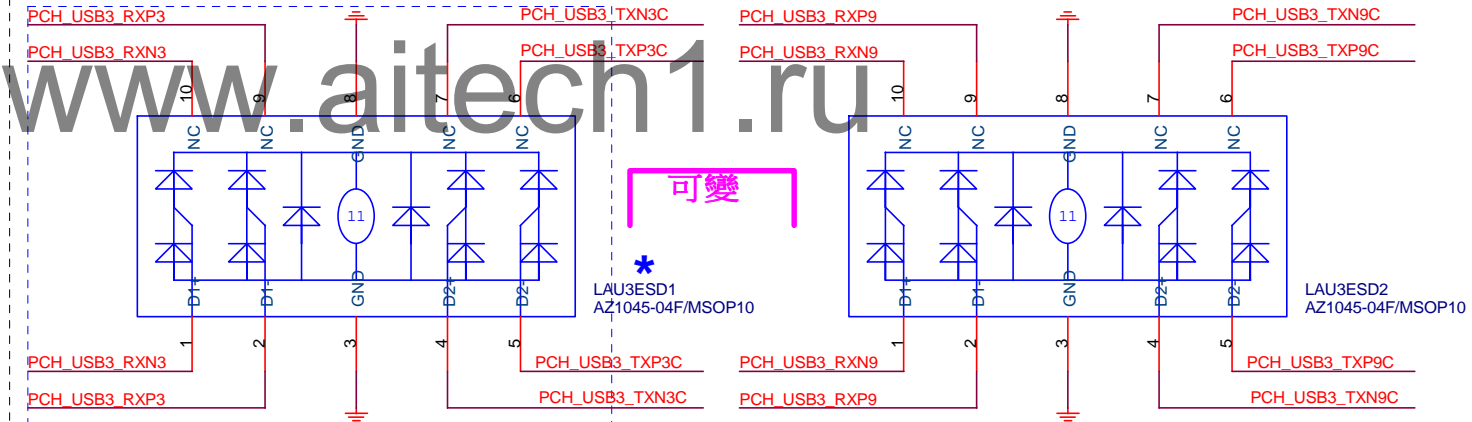
USB_LAN CONNECTOR R1.06



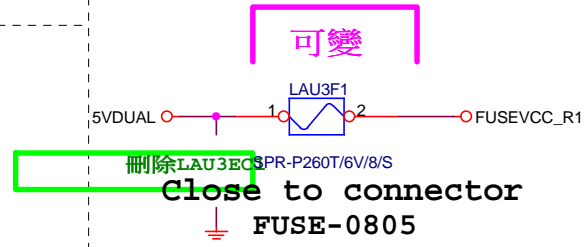
USB30 LAN LAYOUT示意圖



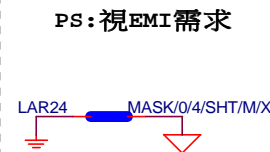
RMA ESD PROTECT



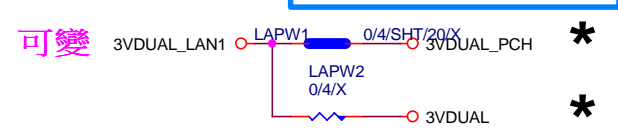
USB POWER



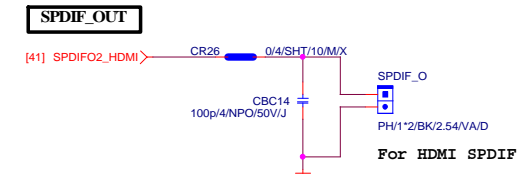
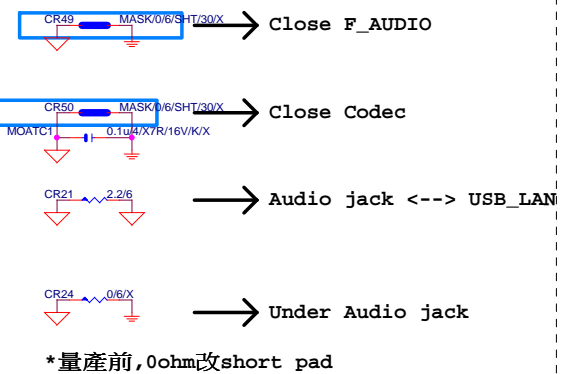
EMI SHORT PAD



LAN POWER

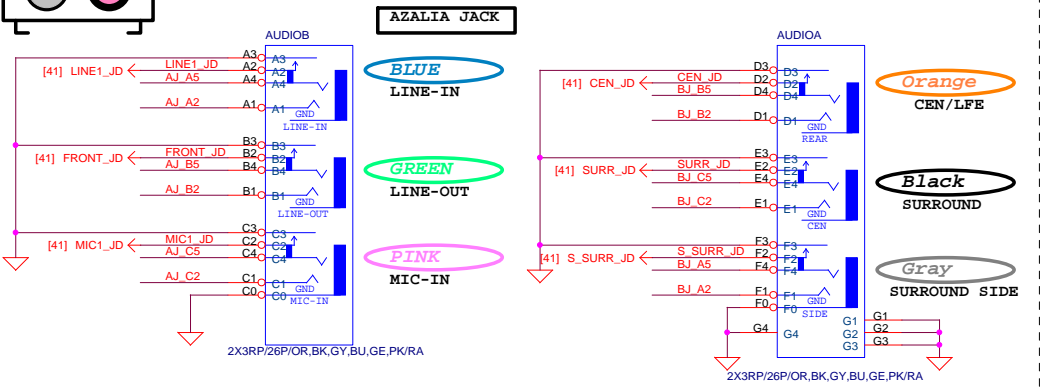
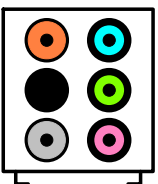


Gigabyte Technology		
LAN CONNECTOR-RTL8111HS		
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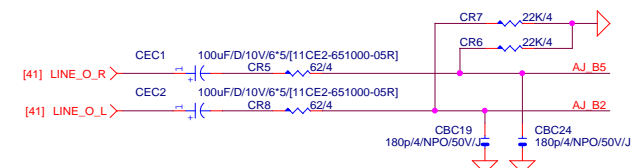


SPDIF_IN

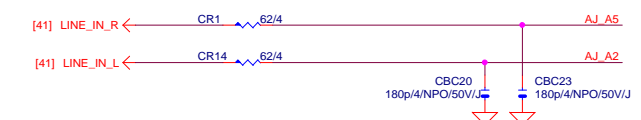
AZALIA JACK



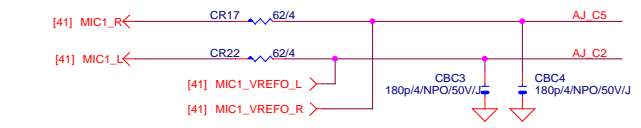
LINE-OUT



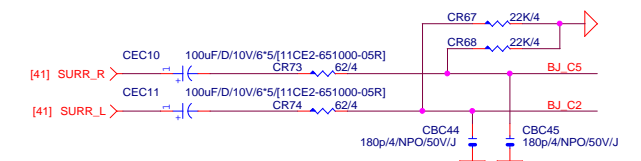
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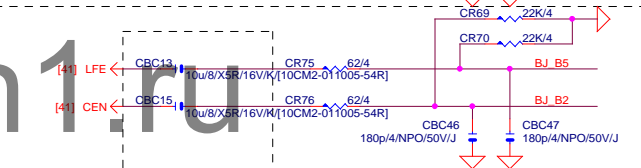
MIC-IN



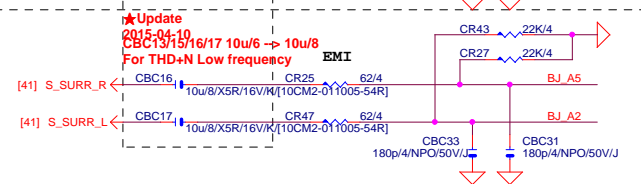
SURROUND



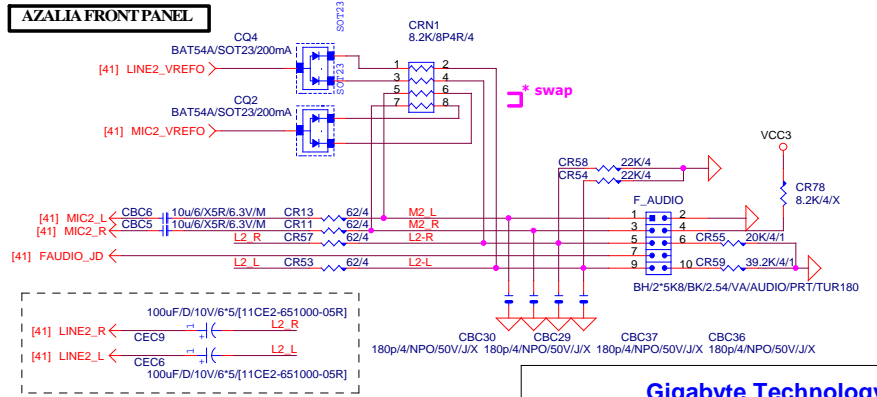
CEN/LFE



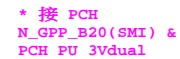
SURRBACK



AZALIA FRONT PANEL

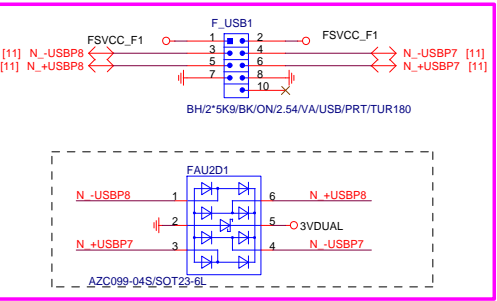


Gigabyte Technology			
Title			
AUDIO JACK			
Size			
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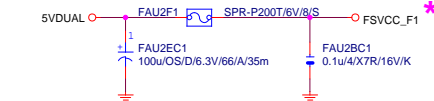


FRONT USB1

NET 可變

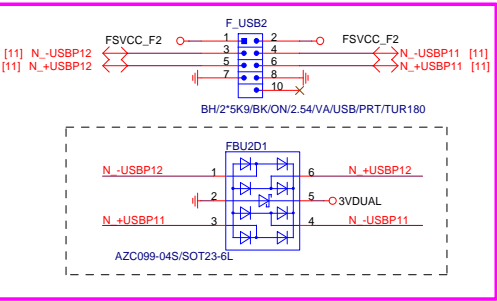


Close to connector
FUSE 2 Port 1 Fuse 2A

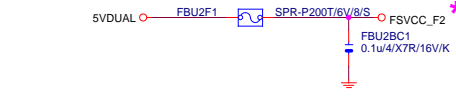


FRONT USB2

NET 可變



Close to connector
FUSE 2 Port 1 Fuse 2A



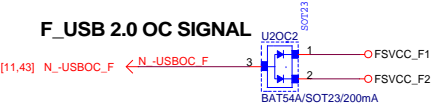
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FRONT USB4

REAR USB1

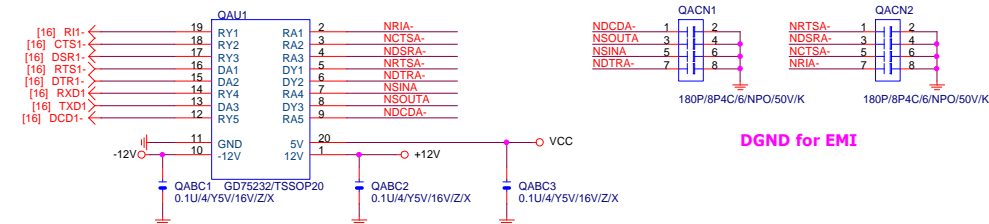
REAR USB2

F_USB 2.0 OC SIGNAL



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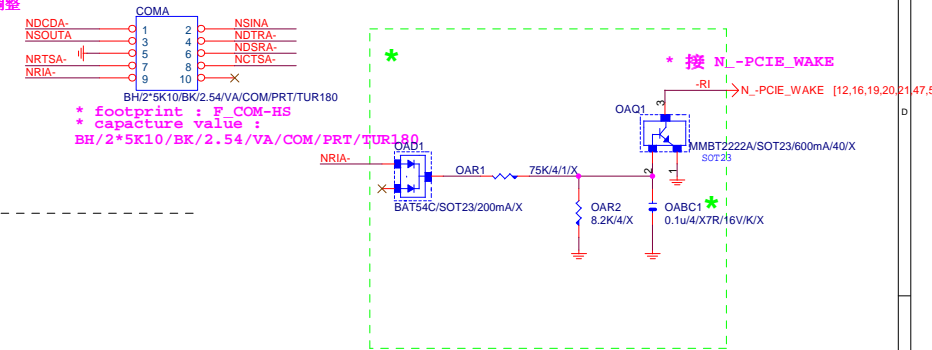
COM PORT



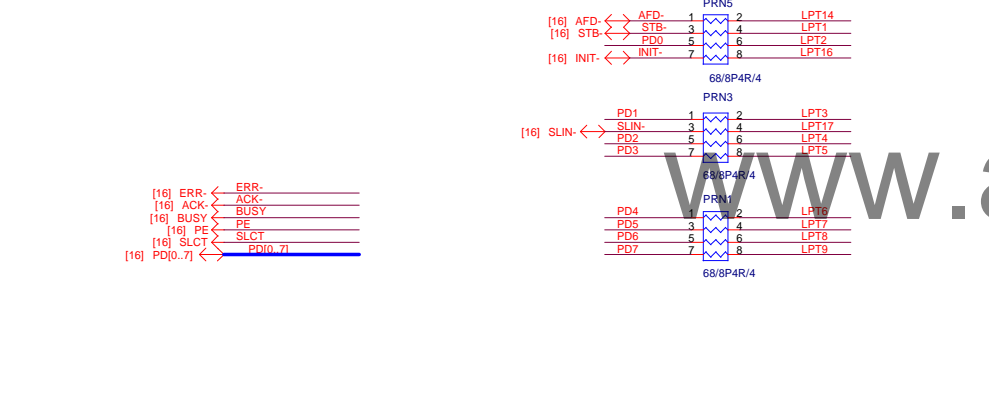
COMA

COMA 自行調整

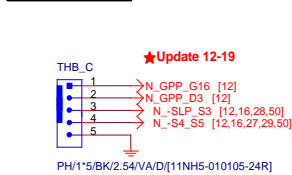
OR



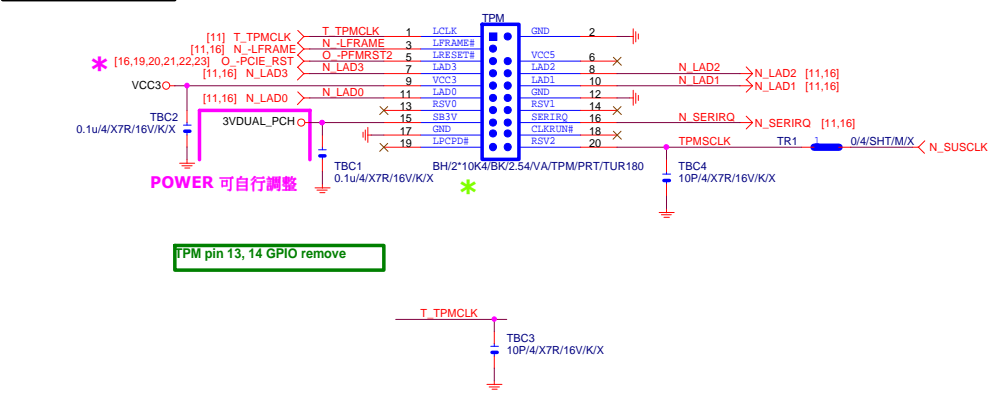
LPT PORT



Thunderbolt

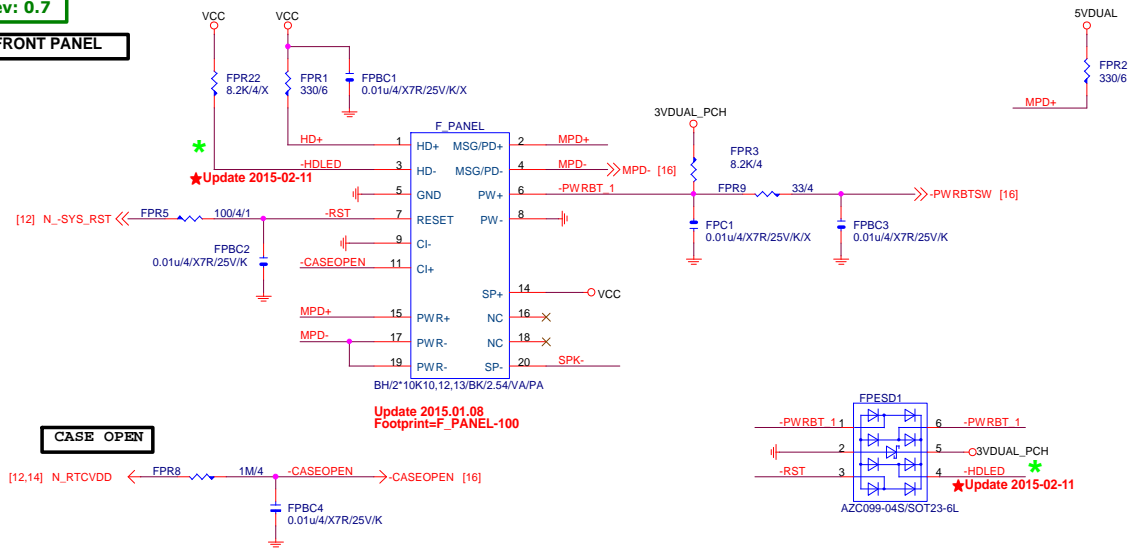


TPM CONNECTOR

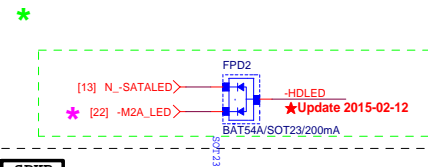


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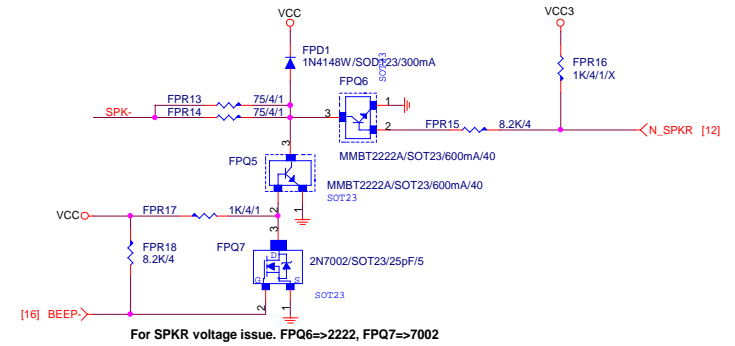
FRONT PANEL



SATA LED

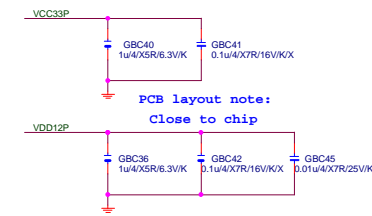
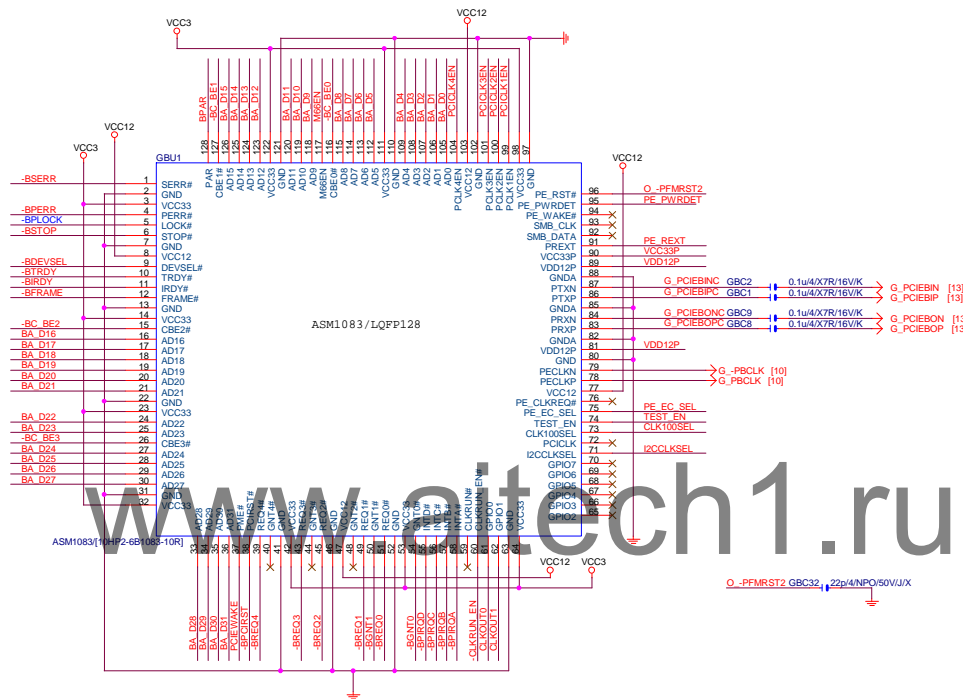
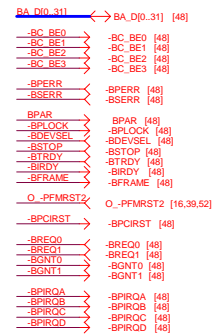
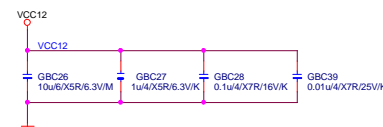
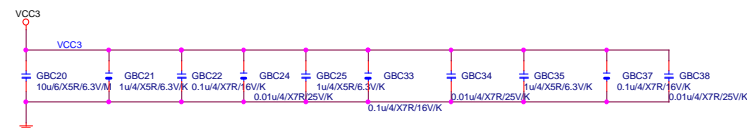


SPKR

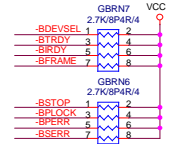
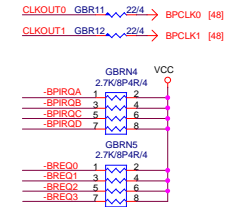


FRONT PANEL SHORT

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PCB layout note:
Close to chip



GBRN4 & GBRN6 swap

CLK100SEL Strapping Set

CLK100SEL	H	L
PCIe CLK	100M +/-N%	100M +/-N%
PCICLK_IN	X	33M
PCICLK0	33M +/-N%	33M

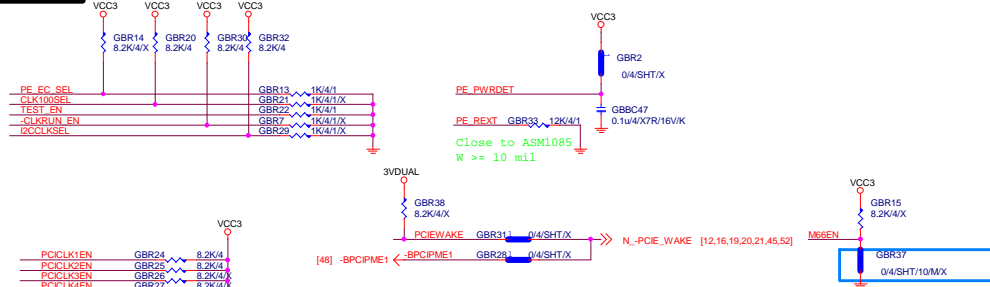
PE_EC_SEL-
 "H" for Express Card mode
 "L" for PCIe Riser Card mode

CLK100SEL-
 "H" for PECLK input only
 "L" for PECLK & PCICLK input

TEST_EN-
 "H" for Test Mode Enable
 "L" for Test Mode Disable

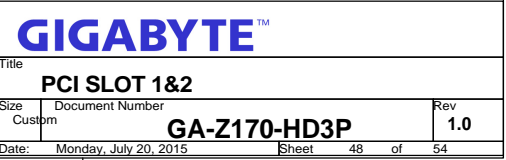
```
-CLKRUN_EN-
"H" for CLKRUN Mode Disable
"L" for CLKRUN Mode Enable
```

```
I2CCLKSEL-
"H" is 135KHz I2CCLK
"L" is 67.5KHz I2CCLK
```

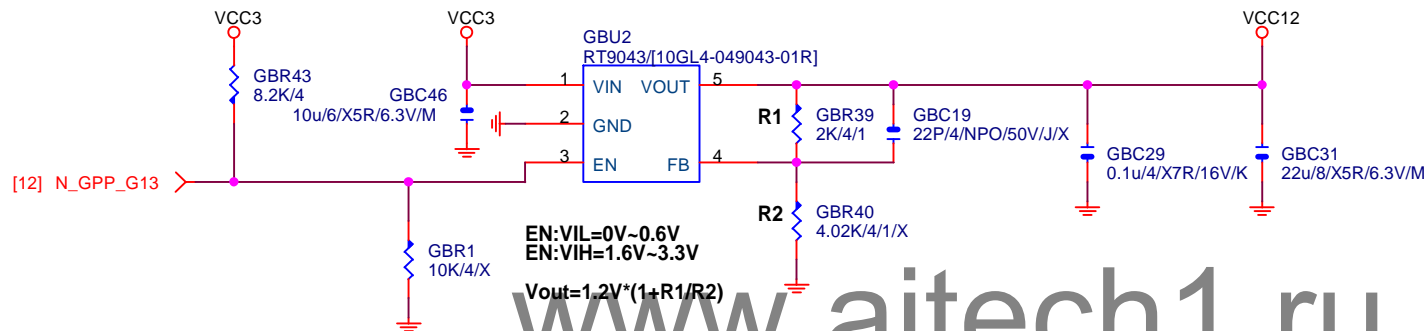


PCI SLOT 1

PCI SLOT 2

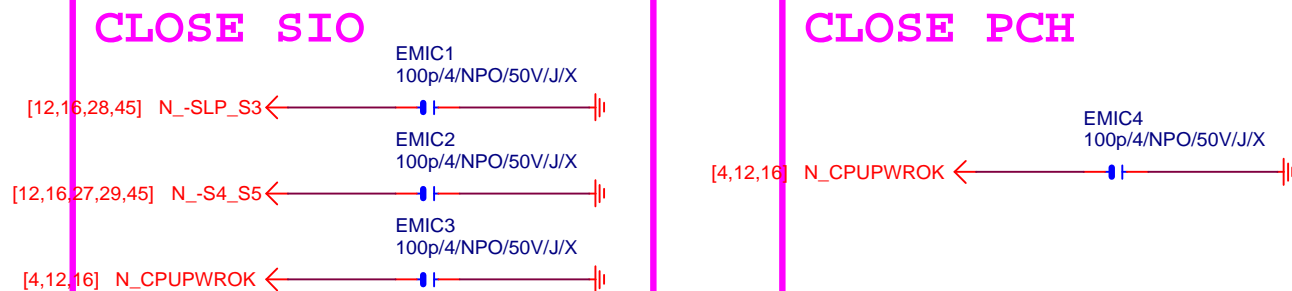


Rev 0.9



Gigabyte Technology

Title			
ASM1085 POWER			
Size	Document Number		Rev
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Title

EMI/ESD

Size
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Document Number

GA-Z170-HD3P

Rev
1.0

Date: Monday, July 20, 2015

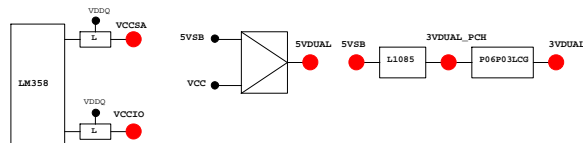
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PCH GPIO LIST TABLE					
PIN NAME	PWR	Default	USAGE	NOTE	
GPP_A0	MAIN	NATIVE	N_KRST	P/U 8.2K VCC3	
GPP_A1	MAIN	NATIVE	N_LAD0	N/A	
GPP_A2	MAIN	NATIVE	N_LAD1	N/A	
GPP_A3	MAIN	NATIVE	N_LAD2	N/A	
GPP_A4	MAIN	NATIVE	N_LAD3	N/A	
GPP_A5	MAIN	NATIVE	N_LFRAME	N/A	
GPP_A6	MAIN	NATIVE	N_SBR1RQ	P/U 8.2K VCC3	
GPP_A7	MAIN	NATIVE	N_LDRQ0	P/U 8.2K 3VDUAL	
GPP_A8	MAIN	NATIVE	N_GPP_A8	P/U 8.2K VCC3	
GPP_A9	MAIN	NATIVE	N_LPC24MB	N/A	
GPP_A10	MAIN	NATIVE	N_LPC24MA	N/A	
GPP_A11	MAIN	NATIVE	N_-P_FMR	P/U 8.2K 3VDUAL_PCH	
GPP_A12	MAIN	GPI	N_GPP_A12	P/U 8.2K VCC3	
GPP_A13	MAIN	NATIVE	N_-S_WARN	N/A	
GPP_A14	MAIN	NATIVE	N_GPP_A14	P/U 8.2K 3VDUAL	
GPP_A15	MAIN	NATIVE	N_-S_ACK	N/A	
GPP_B0	MAIN	CORE_V1D0	N_-DDR_V_SRL	P/U 8.2K VCC3	
GPP_B1	MAIN	CORE_V1D1	N/A	N/A	
GPP_B2	MAIN	GPI	N_-VREALRT	P/U 8.2K 3VDUAL	
GPP_B5	MAIN	GPI	-PCIEIX1_6_PR	P/U 8.2K VCC3	
GPP_B6	MAIN	GPI	-PCIEIX1_PR1	P/U 8.2K VCC3	
GPP_B7	MAIN	GPI	-PCIEIX1_PR2	P/U 8.2K VCC3	
GPP_B8	MAIN	GPI	-PCIEIX4_PR	P/U 8.2K VCC3	
GPP_B9	MAIN	GPI	N/A	N/A	
GPP_B10	MAIN	GPI	N/A	N/A	
GPP_B11	MAIN	GPO	N/A	N/A	
GPP_B12	MAIN	SLP_S0	N_SLP_S0	N/A	
GPP_B13	MAIN	PLTRST	N_-PFRST	N/A	
GPP_B14	MAIN	H-Z	GPO	N_SFRR	N/A
GPP_B18	MAIN	H-Z	GPO	N_GPP_B18	P/D 1K GND
GPP_B20	MAIN	GPI	N_GPP_B20	P/U 8.2K 3VDUAL	
GPP_B22	MAIN	GPI	N_GPP_B22	P/D 1K GND	
GPP_C0	MAIN	SMCLK	N/A	N/A	
GPP_C1	MAIN	SMMDATA	N/A	N/A	
GPP_C2	MAIN	H-Z	GPO	N_-LPCVME	N/A
GPP_C3	MAIN	SMCLK	N_SMLCLK	P/U 499 3VDUAL	
GPP_C4	MAIN	SMCLK	N_SMLCLK	P/U 499 3VDUAL	
GPP_C5	MAIN	H-Z	GPO	N_GPP_C5	N/A
GPP_C6	MAIN	GPI	N_SMLCLK	P/U 8.2K 3VDUAL	
GPP_C7	MAIN	GPI	N_SMLCLK	P/U 8.2K 3VDUAL	
GPP_D4	MAIN	GPI	N_GPP_D4	P/U 8.2K 3VDUAL	
GPP_D7	MAIN	GPI	N_GPP_D7	N/A	
GPP_D9	MAIN	GPI	N_GPP_D9	N/A	
GPP_D17	MAIN	GPI	N_GPP_D17	P/U 8.2K VCC3	
GPP_D18	MAIN	GPI	N_GPP_D18	P/U 8.2K VCC3	
GPP_D19	MAIN	GPI	N_GPP_D19	P/U 8.2K VCC3	
GPP_D20	MAIN	GPI	N_GPP_D20	P/U 8.2K VCC3	
GPP_D23	MAIN	GPI	N_GPP_D23	P/U 8.2K 3VDUAL	
GPP_E0	MAIN	NATIVE	N_GPP_E0	P/U 8.2K VCC3	
GPP_E1	MAIN	NATIVE	N_GPP_E1	P/U 8.2K VCC3	
GPP_E2	MAIN	NATIVE	N_GPP_E2	P/U 8.2K VCC3	
GPP_E3	MAIN	GPI	N_CPU_S	P/U 8.2K VCC3	
GPP_E4	MAIN	GPI	N_DEVSLP0	P/U 8.2K VCC3	
GPP_E6	MAIN	GPI	N_DEVSLP2	P/U 8.2K VCC3	
GPP_E7	MAIN	GPI	N_GT_S	P/U 8.2K VCC3	
GPP_E8	MAIN	GPI	N_-SATALED	N/A	
GPP_E9	MAIN	H-Z	GPI	N_-USB0C_F	N/A
GPP_E10	MAIN	H-Z	GPI	N_-USB0C_R	N/A
GPP_E11	MAIN	H-Z	GPI	N_-USB0C_R	N/A
GPP_E12	MAIN	H-Z	GPI	N_-USB0C_F	N/A
GPP_F0	MAIN	NATIVE	N_GPP_F0	P/U 8.2K VCC3	
GPP_F1	MAIN	NATIVE	N_GPP_F1	P/U 8.2K VCC3	
GPP_F2	MAIN	NATIVE	N_GPP_F2	P/U 8.2K VCC3	
GPP_F3	MAIN	GPI	N_GPP_F3	P/U 8.2K VCC3	
GPP_F4	MAIN	GPI	N_GPP_F4	P/U 8.2K VCC3	
GPP_F5	MAIN	GPI	N_GPP_F5	P/U 8.2K VCC3	
GPP_F6	MAIN	GPI	N_DEVSLP4	P/U 8.2K VCC3	
GPP_F10	MAIN	GPI	N_GPP_F10	P/U 8.2K VCC3	
GPP_F11	MAIN	GPI	N_GPP_F11	P/U 8.2K VCC3	
GPP_F12	MAIN	GPI	N_GPP_F12	P/U 8.2K VCC3	
GPP_F13	MAIN	GPI	N_GPP_F13	P/U 8.2K VCC3	
GPP_F14	MAIN	GPI	A_-SKTOCC	P/U 8.2K VCC3	
GPP_F15	MAIN	GPI	N_-USB0C_F	N/A	
GPP_F16	MAIN	GPI	N_-USB0C_F	N/A	
GPP_F17	MAIN	GPI	N_-USB0C_R	N/A	
GPP_F18	MAIN	GPI	N_-USB0C_F	P/U 8.2K 3VDUAL	
GPP_F22	MAIN	GPI	N_GPP_F22	P/U 8.2K VCC3	
GPP_F23	MAIN	GPI	N_GPP_F23	P/U 8.2K VCC3	
GPP_G0	MAIN	GPI	N_GPP_G0	P/U 1K VCC3	
GPP_G1	MAIN	GPI	N_GPP_G1	P/U 1K VCC3	
GPP_G12	MAIN	GPI	N_GPP_G12	P/U 3.3K VCC3	
GPP_G16	MAIN	GPI	N_GPP_G16	N/A	
GPP_G18	MAIN	GPI	N_GPP_G18	P/U 8.2K VCC3	
GPP_G19	MAIN	GPI	N_GPP_G19	P/U 8.2K VCC3	
GPP_G20	MAIN	GPI	N_GPP_G20	P/U 8.2K VCC3	
GPP_G21	MAIN	GPI	N_GPP_G21	P/U 8.2K VCC3	
GPP_G22	MAIN	GPI	N_GPP_G22	P/U 8.2K VCC3	
GPP_H0	MAIN	GPI	M2_-CLKREQ	P/U 8.2K VCC3	
GPP_H12	MAIN	GPO	N_GPP_H12	P/U 8.2K VCC3	
GPP_H19	MAIN	GPI	N_GPP_H19	P/U 8.2K 3VDUAL	
GPP_H20	MAIN	GPI	N_GPP_H20	P/U 8.2K 3VDUAL	
GPP_H21	MAIN	GPI	N_GPP_H21	P/U 8.2K 3VDUAL	
GPP_H22	MAIN	GPI	N_GPP_H22	P/U 8.2K 3VDUAL	
GPP_I0	MAIN	GPI	N_HDMI_HDP_F	N/A	
GPP_I1	MAIN	GPI	N_DVI_HDP_F	P/U 1M VCC3	
GPP_I2	MAIN	GPI	N_VGA_HDP_F	N/A	

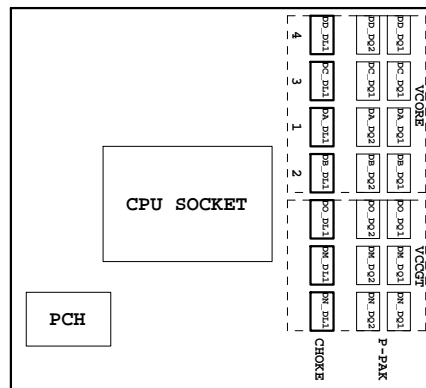
PIN NAME	PWR	Default	USAGE	NOTE
GPP_I3	MAIN	GPI	N_GPP_I3	P/U 8.2K VCC3
GPP_I4	MAIN	GPI	N_GPP_I4	P/D 100K GND
GPP_I5	MAIN	GPI	N_DDPB_CTRLCLK	P/U 2.2K VCC3
GPP_I6	MAIN	GPO	N_DDPB_CTRLCLK	P/U 2.2K VCC3
GPP_I7	MAIN	GPI	N_DDPB_CTRLCLK	P/U 2.2K VCC3
GPP_I8	MAIN	GPI	N_DDPB_CTRLCLK	P/U 2.2K VCC3
GPP_I9	MAIN	GPI	N_DDPB_CTRLCLK	P/U 2.2K VCC3
GPP_I10	MAIN	GPI	N_DDPB_CTRLCLK	P/U 2.2K VCC3
GPD0	STBY	BATLOW	N_-BATLOW	P/U 8.2K 3VDUAL_PCH
GPD1	STBY	ACPRESENT	N_GF_D1	P/U 8.2K 3VDUAL_PCH
GPD2	STBY	LAM_MAKE	N_-LAM_MAKE	N/A
GPD3	STBY	PWRBTN	O_PWRBTNS	P/U 8.2K 3VDUAL_PCH
GPD4	STBY	SLP_S3	N_-SLP_S3	N/A
GPD5	STBY	SLP_S4	N_-SLP_S4	N/A
GPD6	STBY	SLP_A	N_-SLP_A	P/U 8.2K 3VDUAL
GPD7	STBY	NATIVE	N_-S_ACK	N/A
GPD8	STBY	SUSCLK	N_SUSCLK	N/A
GPD10	STBY	SLP_S5	N_-SLP_S5	N/A

Super I/O ITE8720 GPIO Table

PIN NAME	USAGE	NOTE
PCIRSTF3#/GP10/VDIMM_STR_EN	N/A	
PCIRSTF2#/GP11	O_-PCIRST_RST	
PCIRSTF1#/GP12	O_-PFRMST2	
SVC/FRC1_RQ7/GP14	TPM_GP14	
SLP_SUS#/PCIRSTIN/CIRTX2/GP15	-PCIRSTIN	
PSI_L/FAN_CLT5/CIRRX2/GP16	N_-THERMTRIP	
R12#/GP17	MB_ID2	
THR_PWM_CTS2#/GP20	N_-THERMTRIP	
IO_SMI#DCD2#/GP21	紫 PIN	
SPI_S1/GP22	BEEP-	
DPWRKOK/CPU_RQ/GP23	N_PCH_DPWRKOK	
FAN_TACS/RTS2#/GP24	紫 PIN	
FAN_TAC4/DSR2#/GP25	FANIO4	
INV_OUT1_SOUT2/GP26	Q_PLED	
INV_IN1/SIN2/GP27	INV_IN1	
ATXPG/GP30	PWOK	
CTS1/GP31	CTS1-	
OCWD13/R11#/GP32	R11-	
OCWD12/DCD1#/GP33	DCD1-	
VTT_PWRGD/GP34	VTT_PWRGD	
VCC18_EN/GP35	VCCIO_EN	
FAN_CTL3/GP36	FANPWM3	
FAN_TAC3/GP37	FANIO3	
3VSB#W#/GP40	紫 PIN	
OCWD11/SIN1/GP41	RXD1	
GP42/SCK/FAN_CTL4	紫 PIN	
PANSW#/GP43	-PWRBTNS	
PWRON#/GP44	O_PWRBTNS	
OCWD10/DSR1#/GP45	DSR1-	
CE2_N/GP47/JP6	CEB_N	
GP50/JP1	紫 PIN	
FAN_CTL2/GP51	FANPWM2	
FAN_TAC2/GP52	FANIO2	
SUSOC/GP53	N_-SA_S5	
PWR#/GP54	N_-LPCVME	
RSMBST#/CIRRX1/GP55	O_-RSMBST	
KCLK/FAN_TAC2#/GP56	KCLK	
MDAT/FAN_CTL6/GP57	MDAT	
KCLK/GP60	KCLK	
KDAT/GP61	KDAT	
KRST#/GP62	N_-KRST	
HOLD_B#/GP63	-SPI_HOLD_B	
HOLD_B#/GP64	-SPI_HOLD_M	
VLD1T_EN/PCH_D0/GP65	紫 PIN	
VCC1_05_EN/GP66	VCC1_0_EN	
GP67	紫 PIN	
USB_FS1/PD0/GP70	PD0	
USB_FS2/PD1/GP71	PD1	
USB_FS3/PD2/GP72	PD2	
USB_FS3/PD3/GP73	PD3	
USB_FS5/PD4/GP74	PD4	
USB_FS6/PD5/GP75	PD5	
USB_FS7/PD7/GP76	PD6	
USB_FS8/PD8/GP77	PD7	
LS_IN1/SLCT/GP80	SLCT	
LS_OUT1/PE/GP81	PE	
LS_IN2/BUSY/GP82	BUSY	
LS_OUT2/ACK#/GP83	ACK-	
IPHONE_CHARGE#/SLIN#/GP84	SLIN-	
OC_IN/INIT#/GP85	INIT-	
OC_OUT/AFD#/GP86	AFD-	
USB_OC4/STB#/GP87	STB-	
DOX_EN/GP90	NA_EN	
PWRLED/GP91	HPD-	
HOLD_OUT/GP92	紫 PIN	
HDLED_IN/GP93	紫 PIN	
PROCHOT#/GP94	-PROCHOT_CON	
CPUPWRGD/GP95	紫 PIN CPUPWRKOK	
PCH_VRMPWRGD/GP96	N_PCH_VRMPWRGD	
VR_RDY/GP97	VR_RDY	



PWM各相位的擺法如下:



BIOS超電壓對應表:

散熱模組料號:

Z1704-HD3 :

PCH :

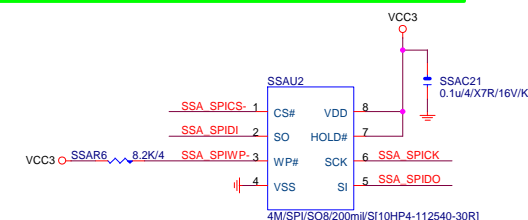
MOSFET :

線路圖名稱	BIOS選項
Vcore	CPU Vcore
VCCGT	CPU Graphic Voltage
VCCSA	CPU System Agent Voltage
VCCIO	CPU I/O Voltage
VCC1_0_PCH	CPU Vcore
VDDQ	DRAM Voltage
VPP_25V	DRAM VPP Voltage
DDRVTT	DRAM Termination
VREF_DQ_AVREF_DQ_B	DRAM Data Ref

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	+12V	FANPWM1	FANIO1	IT8628
SYS FAN1	FANPWM2	VCC	FANIO2	IT8628
	FAN1_VOUT	N/A	N/A	NCT3941
SYS FAN2	FANPWM3	VCC	FANIO3	IT8628
	FAN2_VOUT	N/A	N/A	NCT3941
SYS FAN3	+12V	N/A	FANIO4	IT8628

ASM1142 USB3.1

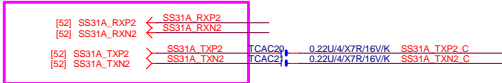
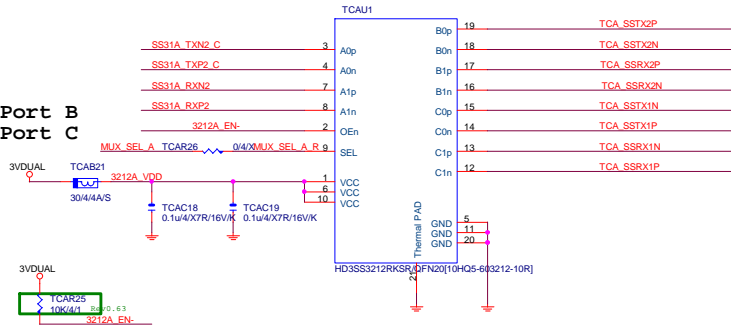
Base on ASM1142 0.3 Reference SCH



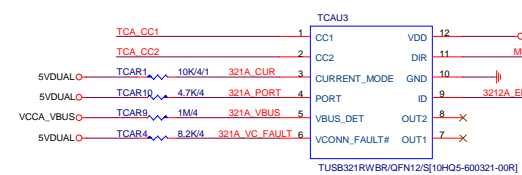
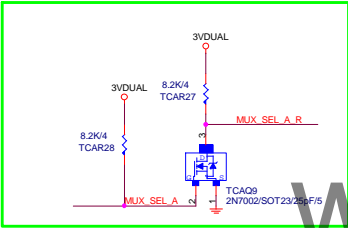
Title			
ALPINE RIDGE CIO & DP			
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SEL
L - Port A to Port B
H - Port A to Port C



USB 3.x SuperSpeed

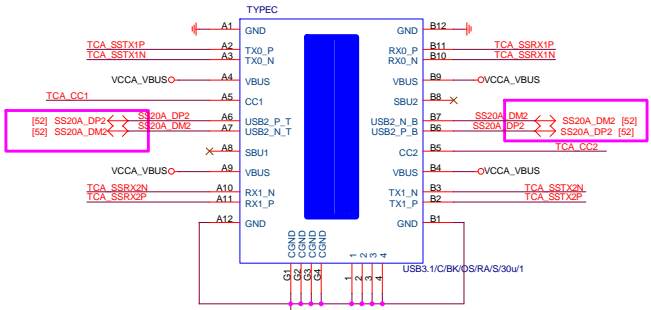


MUX_SEL
H - TypeC plug position 2
L - TypeC plug position 1

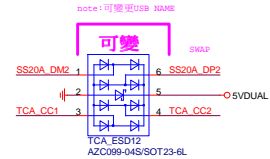
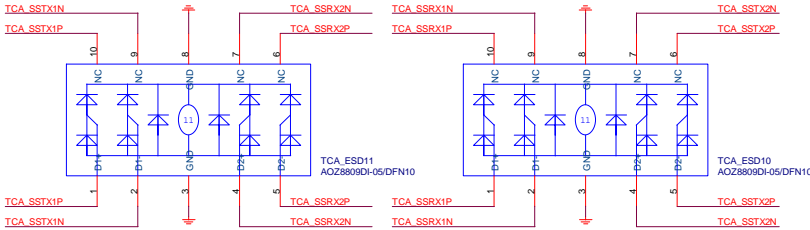
CURRENT MODE
L - Default current / Pull down to GND or NC
M - Medium (1.5A) current / Pull up to VDD 500K
H - High (3.0A) current / Pull up to VDD 10K

PORT
H - HOST
L - Device
NC - Dual
Role

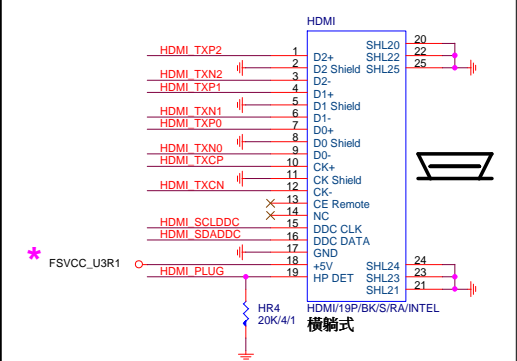
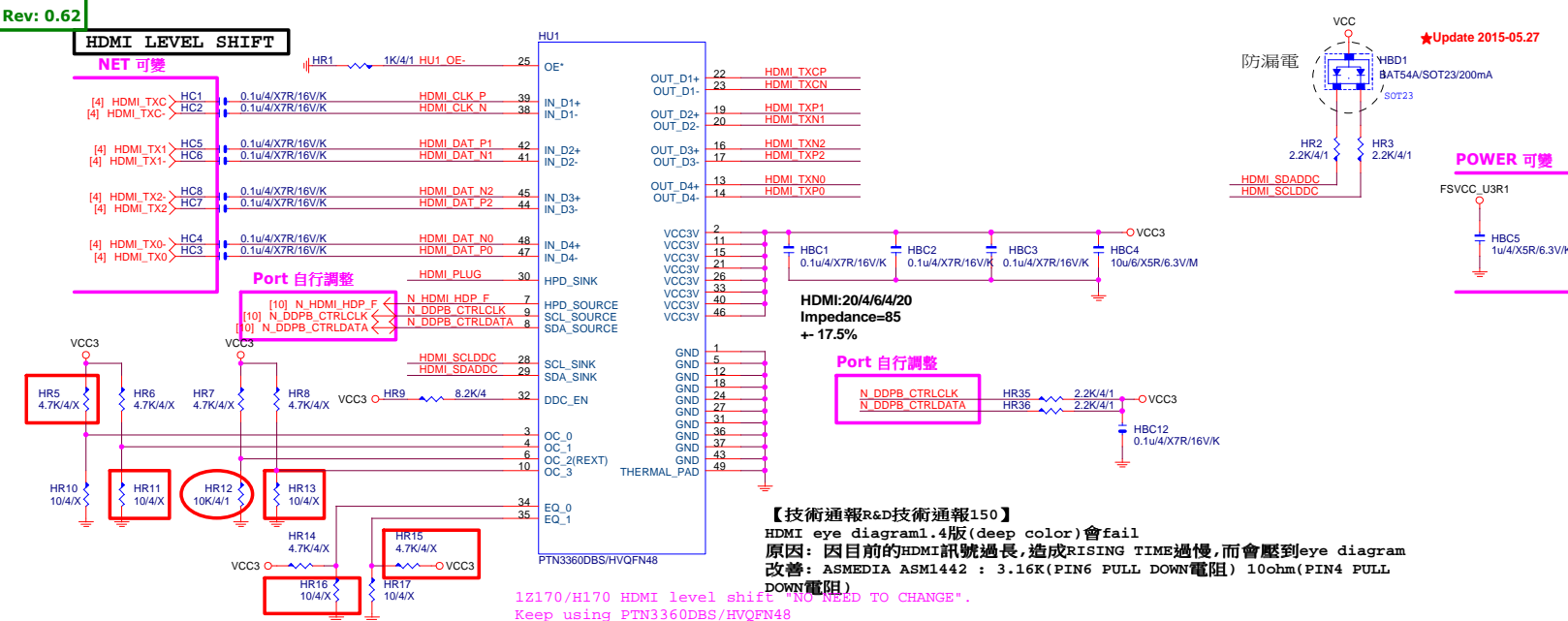
Color markers can be changed by model



USB2.0 can be used the same source



GIGABYTE™		
HD3SS3212&TUSB321_A		
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PTN3360:PIN 4/10/34/35 NC PIN,都不上值;只上HR12:10K
ASM1442:紅色框要上,HR12:3.16K

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